In-Situ De-embedding (ISD)

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Outline

- 什么是因果关系
- 生么是原位去嵌入(ISD)
- ISD与仿真及其他软件的比较
- 非因果去嵌入如何影响连接器一致性测试
- 如何提取没有尖峰和毛刺的准确的PCB走线线衰减
- 如何通过匹配去嵌入的PCB走线的所有IL，RL，NEXT，FEXT和TDR / TDT特性来提取PCB的材料属性（DK，DF，粗糙度)

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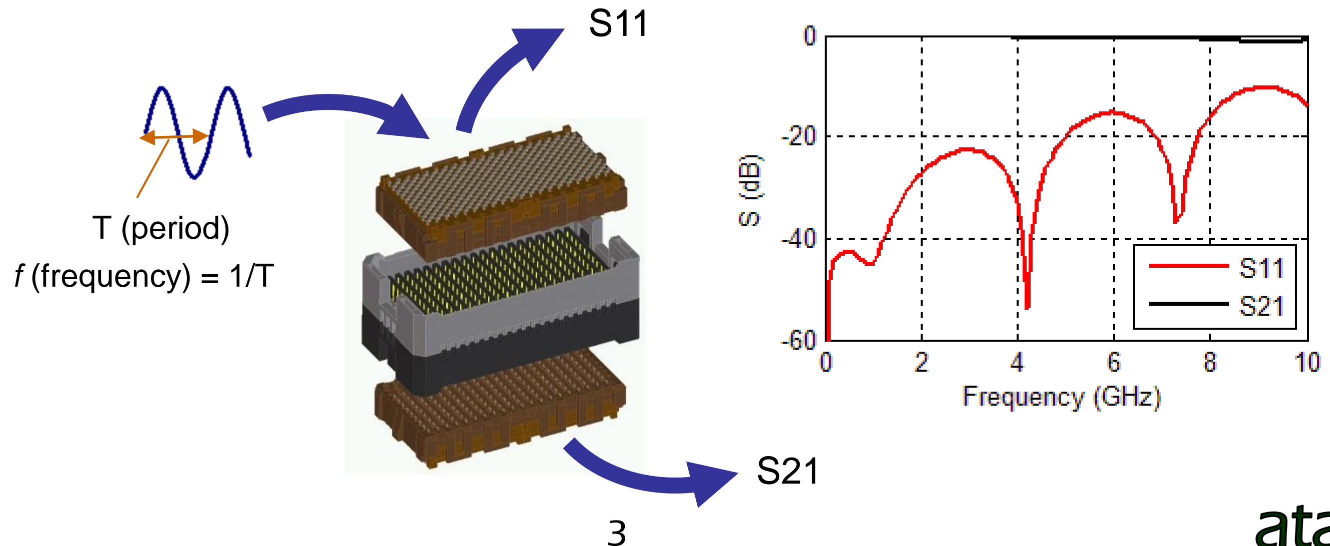
VNA and S parameter

- 网络络分析仪（VNA）是一种将正弦波发射到某种结构中，改变波形的周期（或频率）使我们能够观察传输波和反射波的"频域响应"的设备
- 当将这种频域响应归一化为入射波时，称为散射参数（或S参数）



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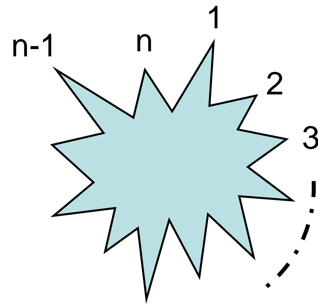
What is S parameter

- 对于n端口（或I / O）设备，S参数为n x n矩阵:



$$[S_{ij}]_{n\times n} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \dots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \dots & S_{2n} \\ \vdots & \vdots & \vdots & & \vdots \\ S_{n1} & S_{n2} & S_{n3} & \dots & S_{nn} \end{bmatrix}$$

- S_{ij} 端口J到端口I的S参数
- S_{ij}具有独特的性质，对于无源设备，其大小小于或等于1（或0 dB)

$$|S_{ij}| \leq 1$$

$$S_{ij}(dB) = 20 \times \log_{10}|S_{ij}| \leq 0 \quad dB$$

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什么是Touchstone (.sNp) 文件

- 每个频率下的S参数以Touchstone文件格式表示

in GHz
S param
in dB and phase angle
Reference impedance

```
! Total number of ports = 4
! Total number of frequency points = 800
# GHZ  S  DB  R  50
0.025  -36.59296  48.77486  -41.40676  79.91354  -0.08648679  -6.544144  -49.50045  -105.618
       -41.39364  79.94686  -36.35592  51.52433  -49.4886  -105.5124  -0.09038406  -6.527076
       -0.08421237  -6.537903  -49.44814  -105.644  -36.0317  49.60022  -41.37105  79.91856
       -49.44393  -105.8186  -0.09834136  -6.542909  -41.36758  79.9318  -36.05645  48.98348
0.05  -32.22576  48.03161  -35.59394  74.15976  -0.1277169  -12.82876  -43.90183  -112.0995
       -35.58736  74.16304  -32.12694  50.92389  -43.90926  -112.0764  -0.132402  -12.7985
       -0.1242117  -12.82302  -43.89  -112.0248  -32.10987  50.3115  -35.56998  74.078
       -43.88424  -112.0517  -0.1381616  -12.80199  -35.56758  74.06782  -31.94136  50.49276
0.075  -29.88861  42.02766  -32.19713  68.06704  -0.1589249  -19.05252  -40.67476  -118.8188
       -32.19116  68.0941  -29.7086  45.41557  -40.63857  -118.837  -0.1635606  -19.01593
       -0.1603356  -19.0376  -40.63557  -118.8543  -29.89064  47.63852  -32.16917  67.94677
       -40.65711  -118.8021  -0.1737256  -19.02956  -32.16865  67.93389  -29.65444  46.15548

    :        :          :
```

Frequency in GHz

S11, S12, …, S44 in dB and phase angle

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什么是因果关系

cau·sal·i·ty

/kôˈzalədē/

noun

1. the relationship between cause and effect.因果关系
2. the principle that everything has a cause.
一切都有原因的原则

In other words:

Can not get something from nothing.

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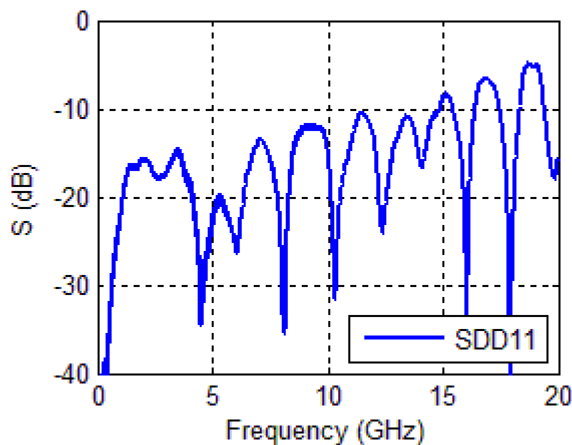
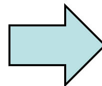
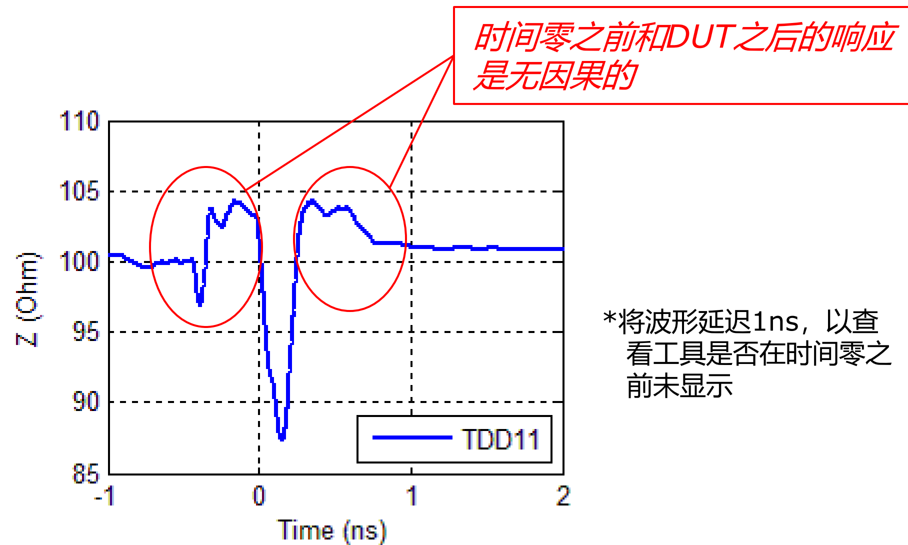
如何识别非因果S参数

- 把S参数转换成TDR/TDT.

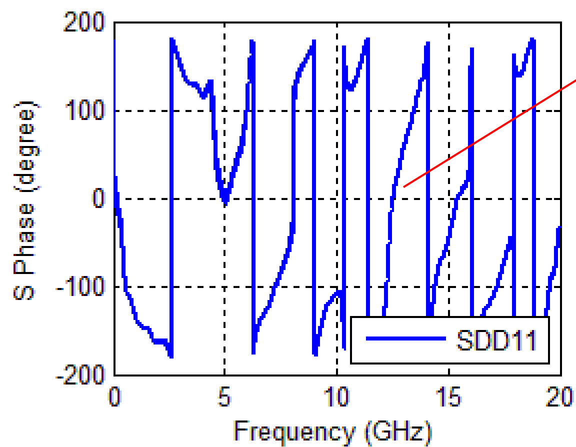






*将波形延迟1ns，以查看工具是否在时间零之前未显示

- 相位.



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为什么S参数违反因果关系

- 测量误差（去嵌入），模拟误差（材料特性）和S参数的有限带宽都造成了非因果关系.
- Kramers-Kronig关系要求解析函数的实部和虚部通过希尔伯特变换相互关联:

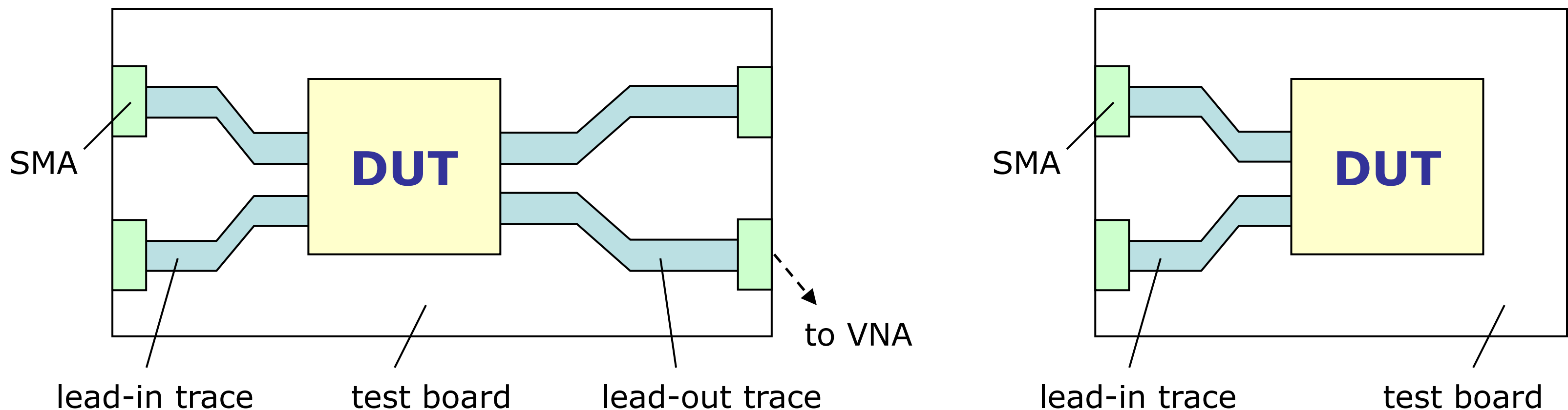
$$\Psi(\omega)=\Psi_R(\omega)+j\Psi_I(\omega)$$

$$\Psi_R(\omega)=\frac{1}{\pi}P\int_{-\infty}^{\infty}\frac{\Psi_I(\omega')}{\omega'-\omega}d\omega'$$

$$\Psi_I(\omega)=-\frac{1}{\pi}P\int_{-\infty}^{\infty}\frac{\Psi_R(\omega')}{\omega'-\omega}d\omega'$$

什么是去嵌入

- 消除夹具（SMA连接器+导入/导出）的影响并提取DUT（被测设备）的S参数



- 引入和引出走线不一定要相同
- 有许多器件甚至没有引入和引出走线(如芯片封装).

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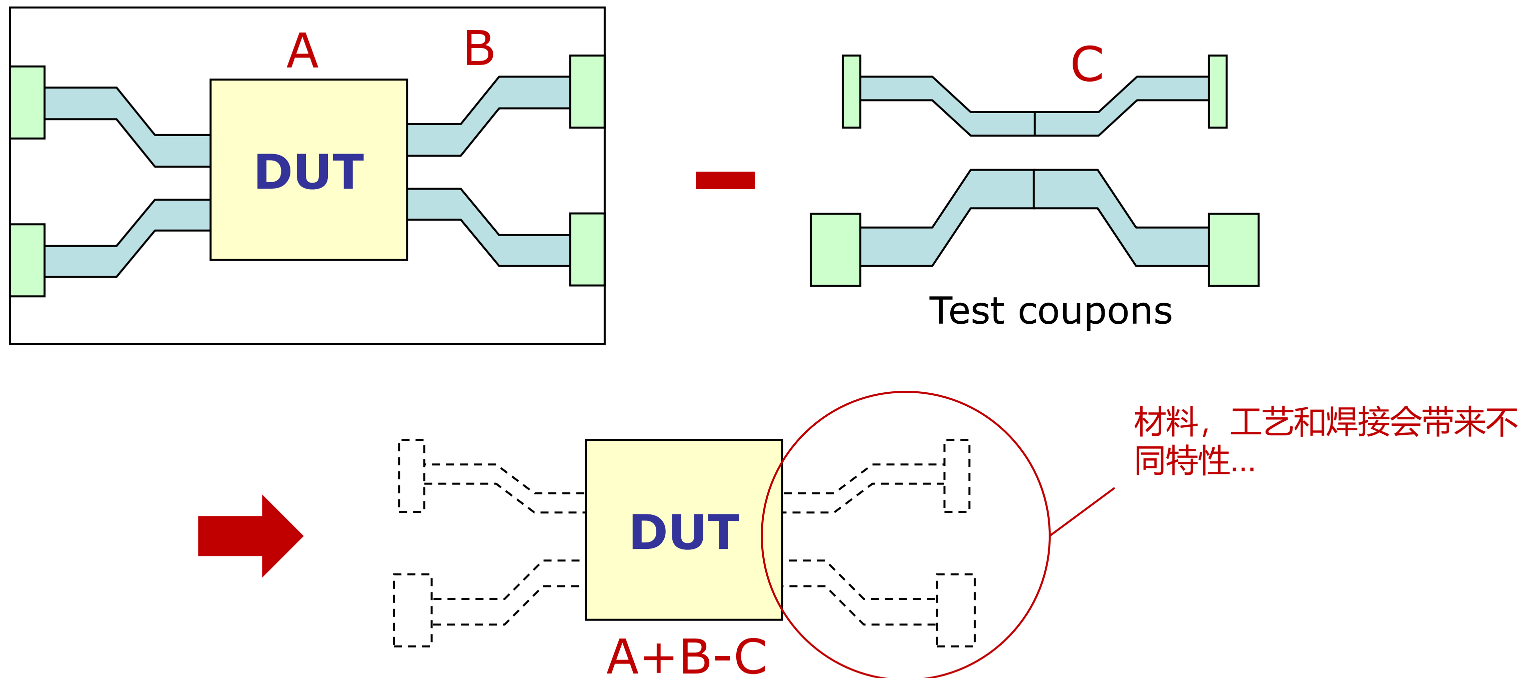
为什么大多数去嵌入工具都会导致因果关系错误

- 大多数工具直接使用测试样板进行去嵌入，因此实际夹具和测试样板之间的差异会累积到DUT结果中。



* http://www.edn.com/electronics-blogs/test-voices/4438677/Software-tool-fixes-some-causality-violations by Eric Bogatin

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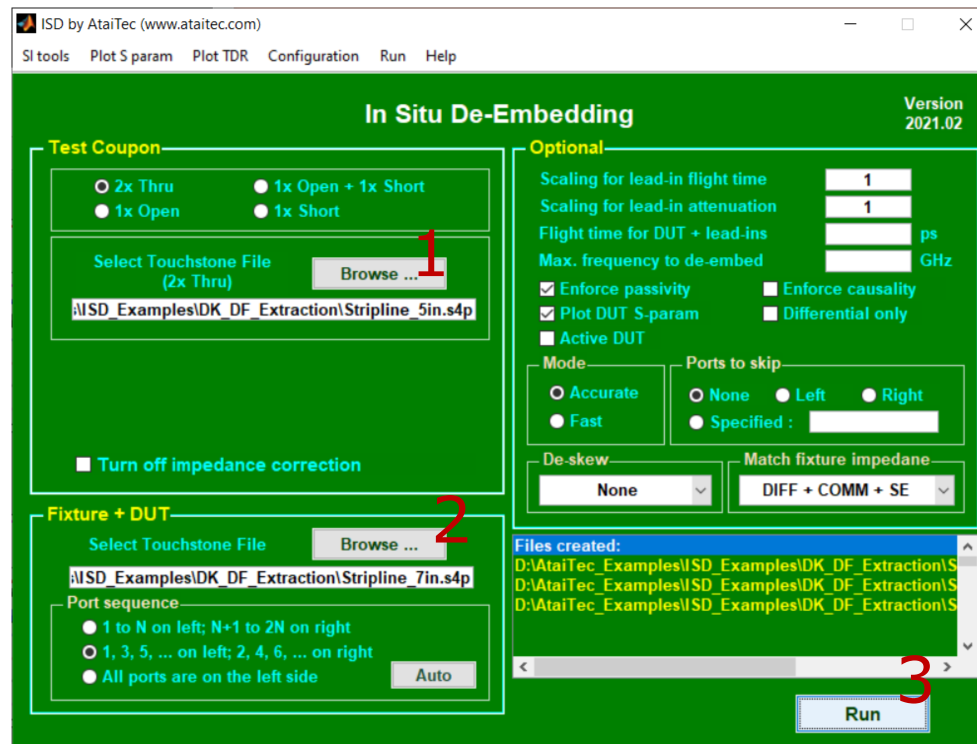
介绍什么是原位去嵌入（ISD）以解决阻抗变化

- ISD使用测试校准件（“ 2x thru”或“ 1x open / 1x short”）作为参考，并通过数值优化对夹具的实际阻抗进行去嵌入
- 其他方法直接使用测试校准件进行去嵌入，而当测试校准件和要去嵌入的实际夹具具有不同的阻抗时，会导致因果关系错误
- ISD通过软件而非硬件解决了测试校准件和实际夹具之间的阻抗变化，从而提高了去嵌入精度并降低了硬件成本。



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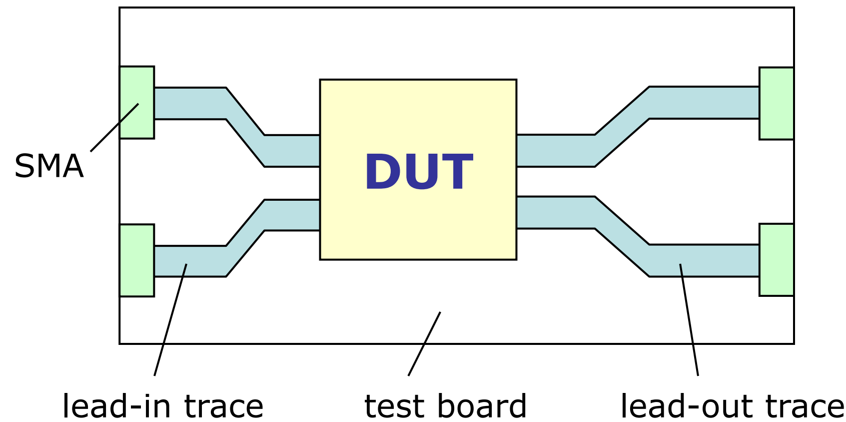
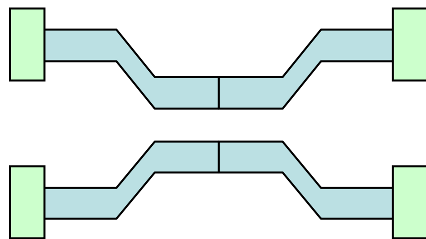
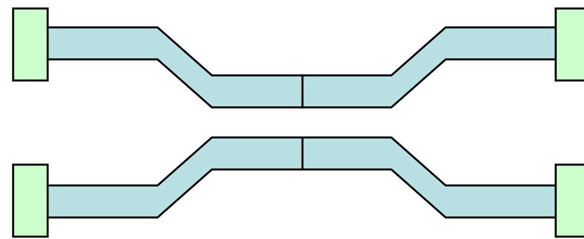
什么是“2x thru”

- “2x thru” 是 2x lead-ins引入走线 或lead-outs引出走线.





2x thru for lead-ins



2x thru for lead-outs

非对称夹具需要2套 “ 2x thru”

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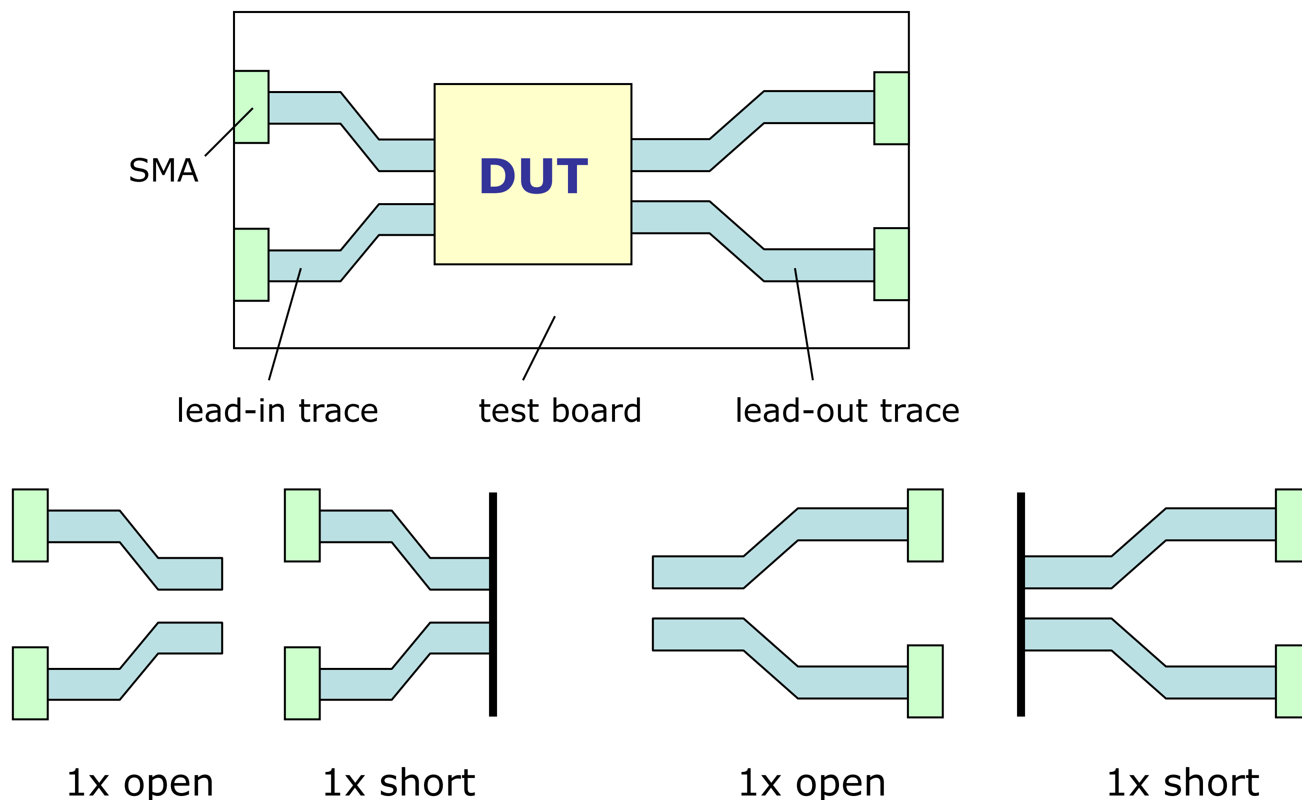
什么是“1x open / 1x short”

- “1x open / 1x short” 是当“2x thru” 不可用时(如连接器，过孔，封装等)采用.



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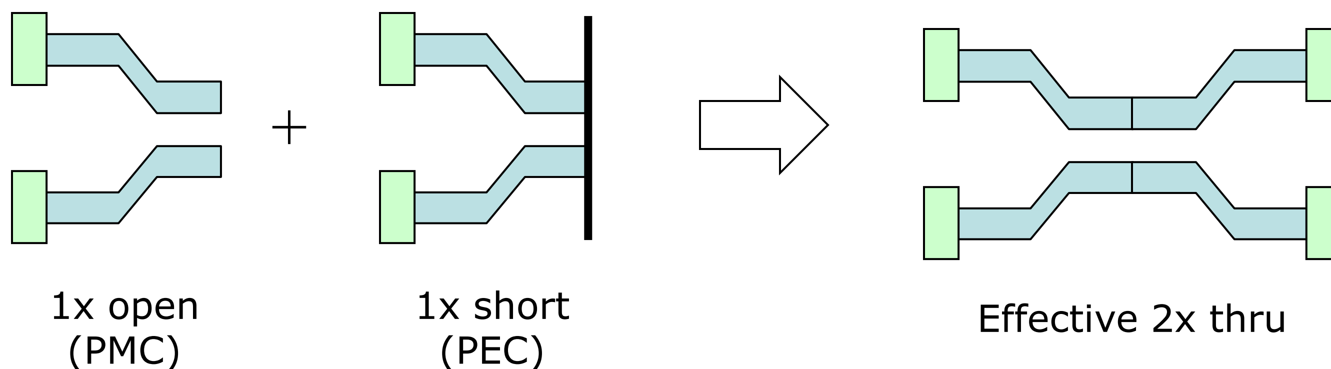
什么是“1x open + 1x short”

- “1x open + 1x short” 可以等效为2x thru.



$$[S]^{2x} = \begin{bmatrix} S_{11}^{2x} & S_{12}^{2x} \\ S_{12}^{2x} & S_{11}^{2x} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} S_{11}^{open} + S_{11}^{short} & S_{11}^{open} - S_{11}^{short} \\ S_{11}^{open} - S_{11}^{short} & S_{11}^{open} + S_{11}^{short} \end{bmatrix}$$

* C.C. Huang, "Fixture de-embedding using calibration structures with open and short terminations," US patent no. 9,797,977, 10/24/2017.可以参考这个专利

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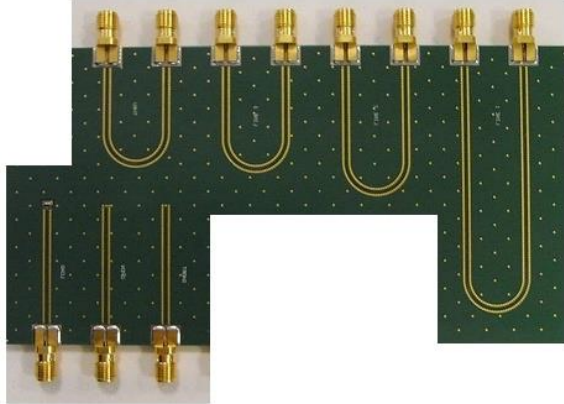
为什么ISD是更精准又经济?

TRL calibration board



- 更大的电路板空间-需要多个测试校准线路.
- 测试校准件直接用于去嵌入
- 校准件和实际DUT板之间的所有差异都会累积到DUT结果中
- 需要优质但昂贵的SMA，PCB材料（Roger）和严格的公差工艺要求-不可能保证所有的连接器和PCB工艺都绝对相同
- 需要耗时的手动校准-参考平面在DUT的前面

ISD test coupon

- 只需一张2xthru 测试校准件.
- 测试校准件仅用于参考，不用于直接去嵌入
- 实际的DUT板阻抗被去嵌入
- 可以采用一般的连接器和PCB材料以及PCB制程工艺
- 电子校准可以用于SOLT 校准.
  - 参考平面在SMA前面
  - 去嵌入仅需要两个输入文件：2xthru和DUT板（SMA至SMA）的Touchstone文件.
  - 更多信息：可以输出去嵌入和DUT文件

* TRL = Thru-Reflect-Line

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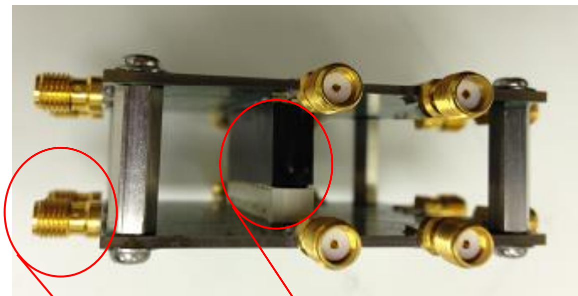
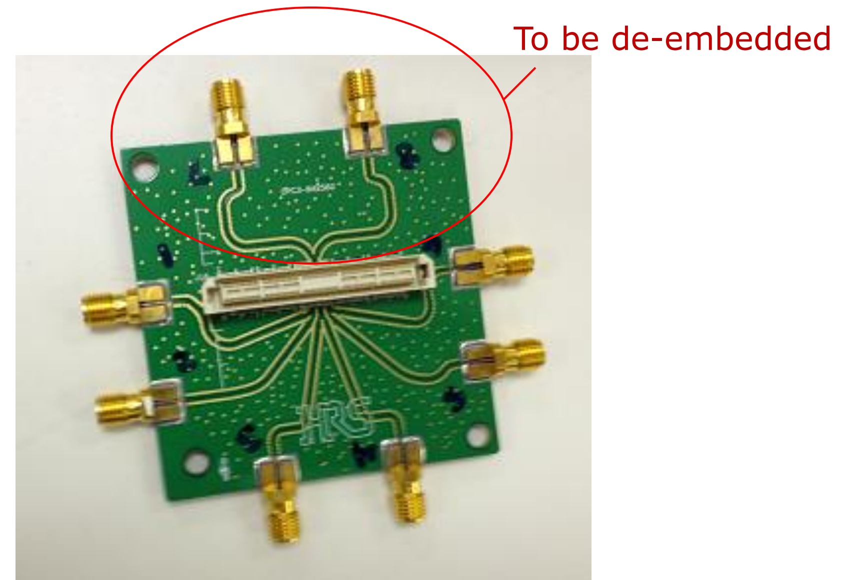
示例1：夹层连接器的测试 ISD与TRL比较

- 在此示例中，我们将使用ISD和TRL提取夹层连接器的性能并比较它们的结果



SMA

Mezzanine connector (DUT)



*Courtesy of Hirose Electric

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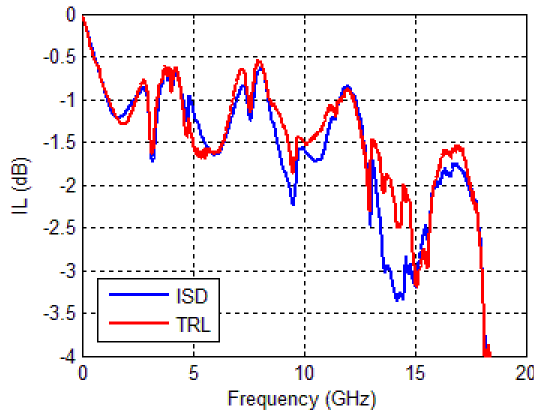
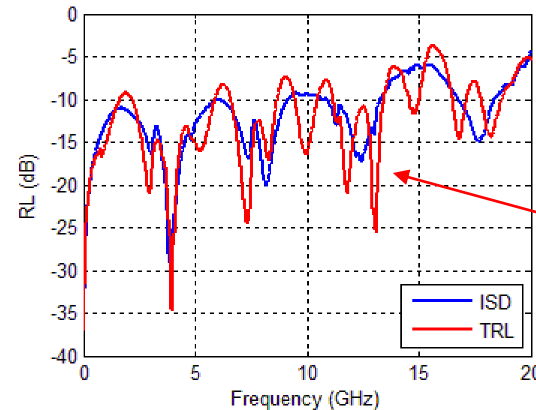
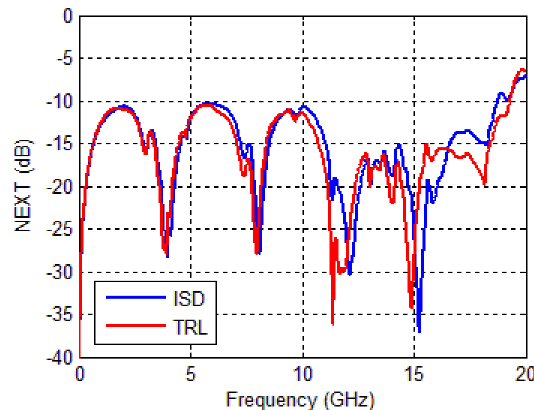
使用ISD和TRL之后的DUT结果哪个更准确?

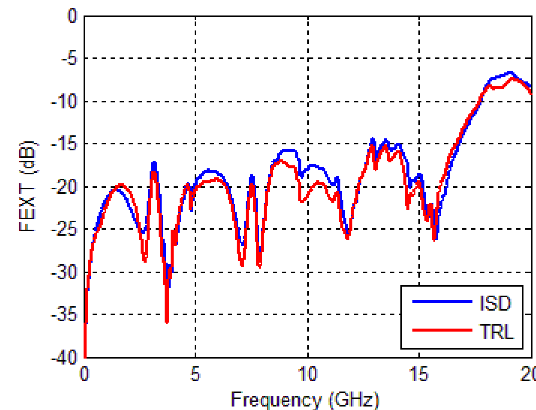
- 对于这么小的DUT，TRL会在回波损耗（RL）中产生过多的纹波





Non-causal ripples





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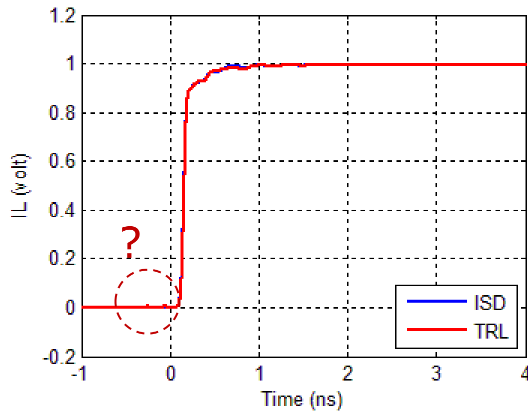
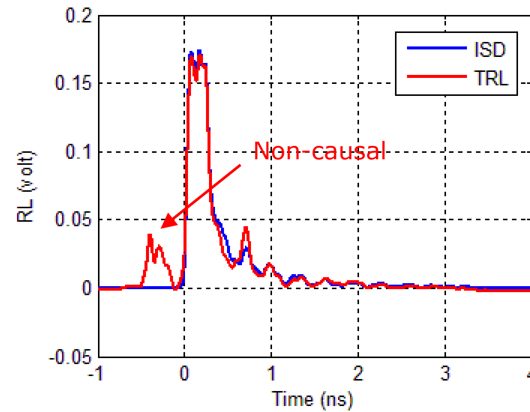
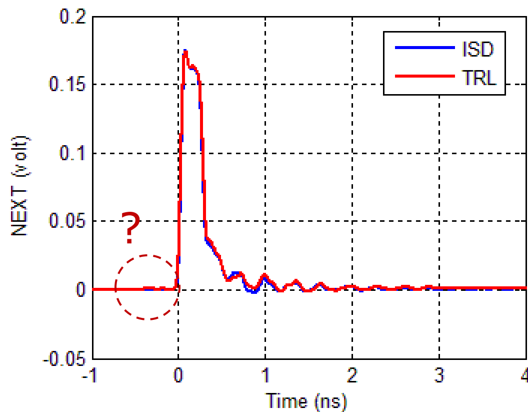
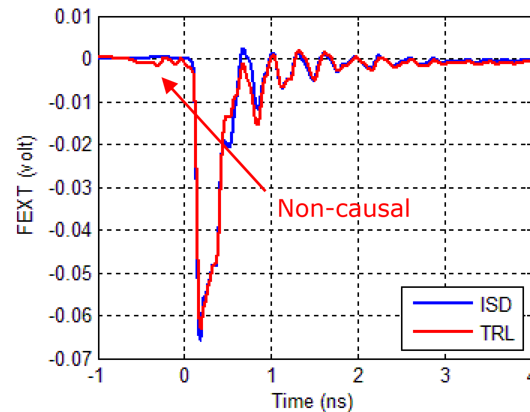
将S参数转换为TDR / TDT显示TRL的方法中有非因果关系的反射









Rise time = 40ps (20/80)

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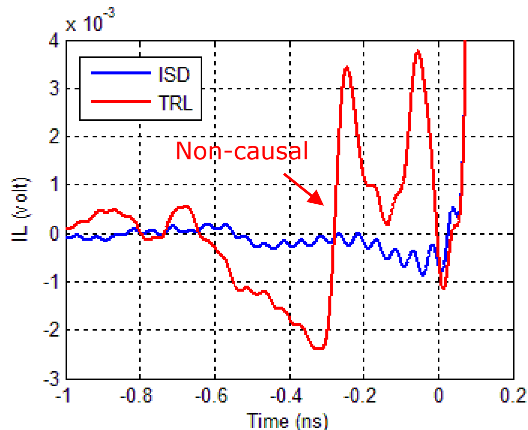
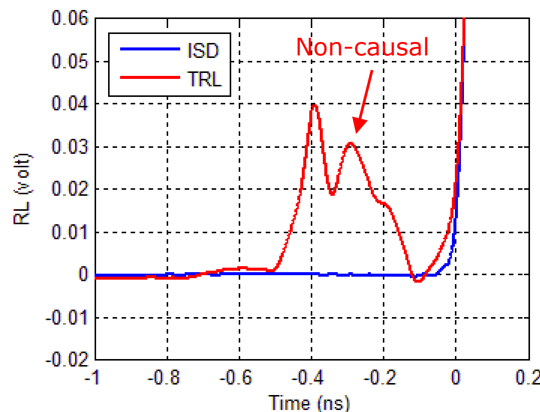
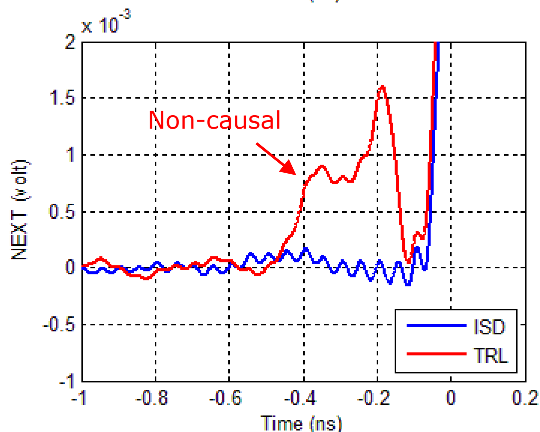
放大显示所有TRL方法中IL，RL，NEXT和FEXT的非因果结果

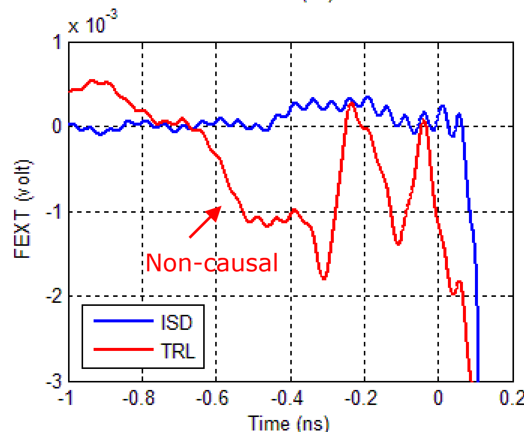
- 在这种情况下，TRL导致时域误差为0.38%（IL），25.81%（RL），1.05%（NEXT）和2.86%（FEXT）*





*使用一位响应和/或更快的上升时间时，该百分比会更大





Rise time = 40ps (20/80)

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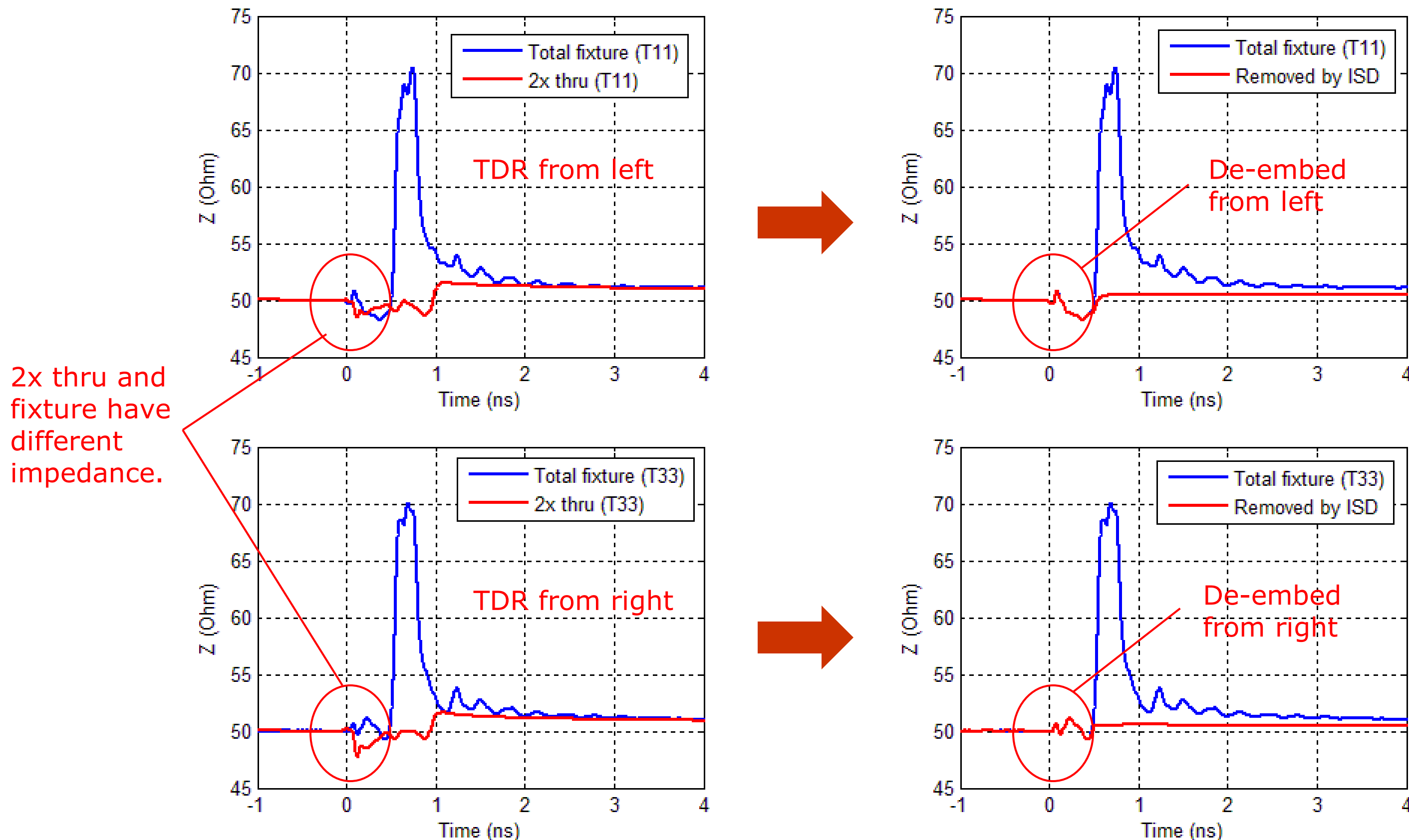
ISD是怎么做的?

- 通过数值优化，ISD可以准确地去嵌入夹具的阻抗，而不受2xThru校准件的阻抗的影响。



Rise time = 40ps (20/80)

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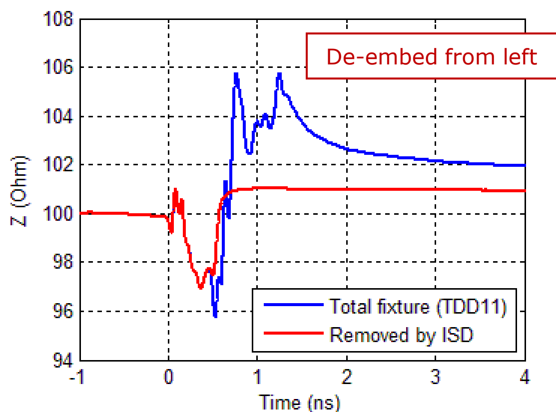
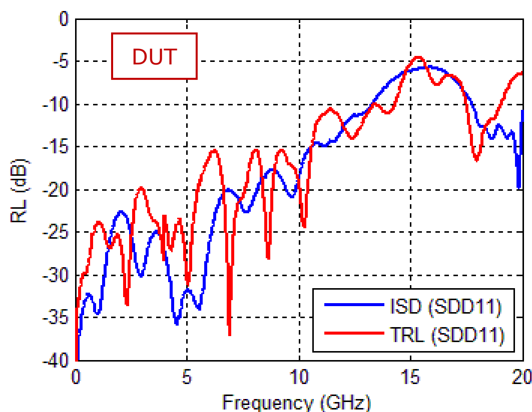
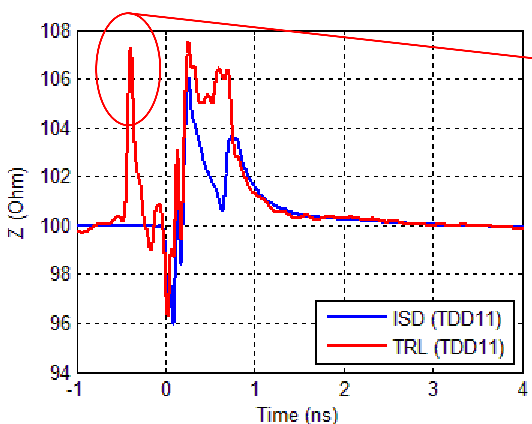
即使阻抗变化很小，TRL也会在SDD11中产生巨大的误差*

- ISD只需单根走线的2xthru校准件即可去嵌入夹具的差分阻抗.







由于违反因果关系，TRL给出了超过100%的错误.

Rise time = 40ps (20/80)

* 2xthru与夹具之间的阻抗变化小于5%。 (请参阅上一张幻灯片)。

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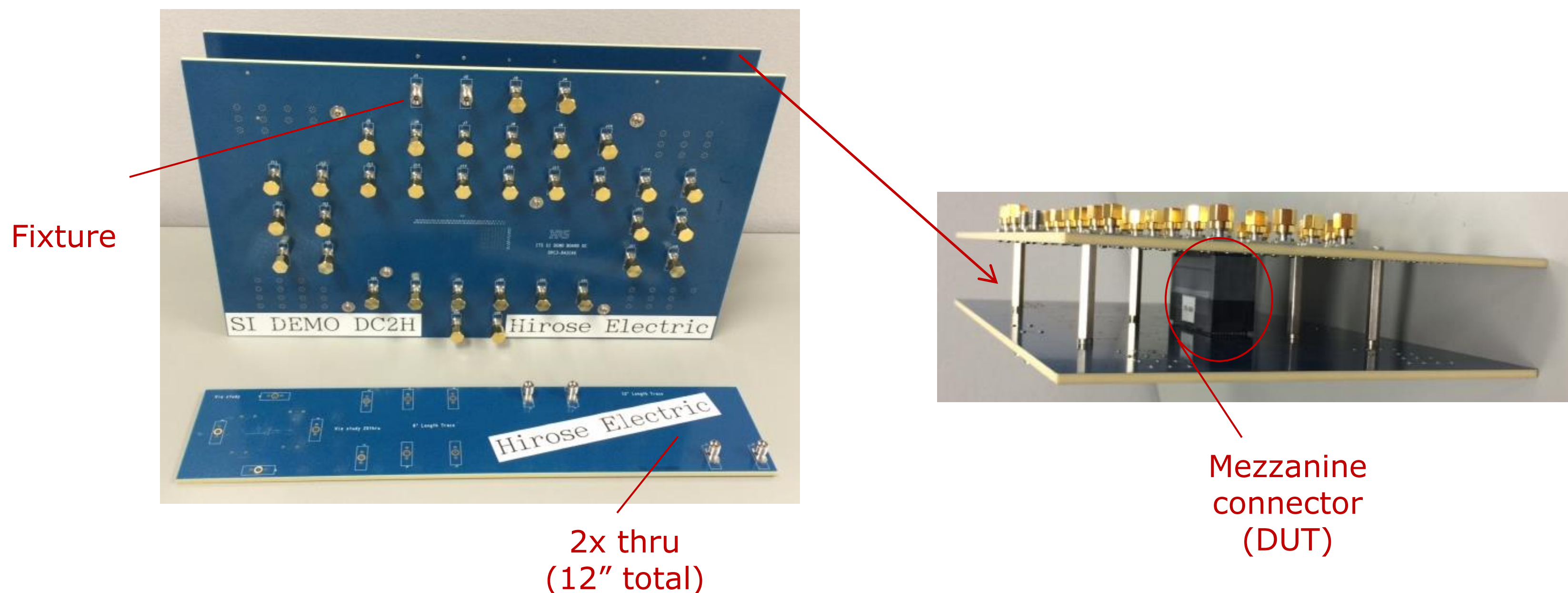
示例2：夹层连接器性能从大板上提取

- TRL对于去嵌入大的和有耦合的引入/引出是不实用的.



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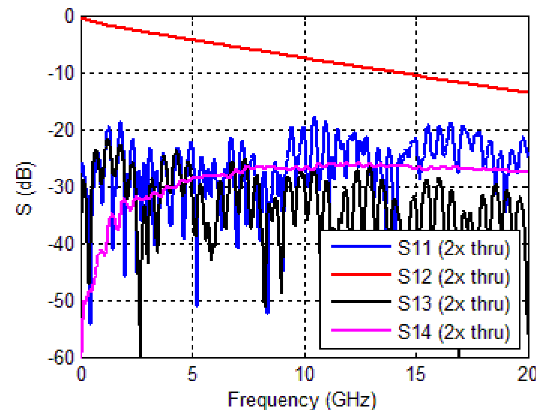
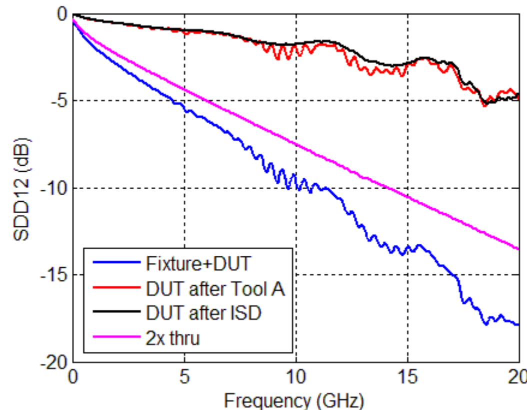
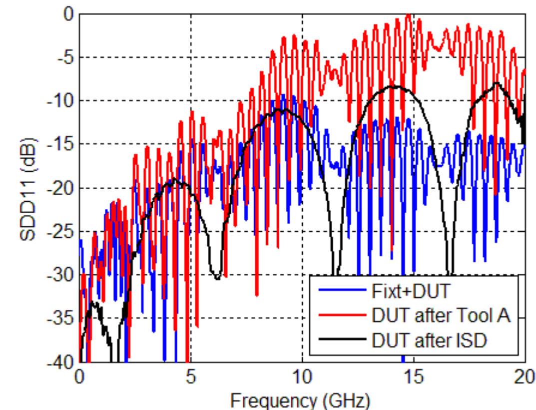
ISD可以使用2xthru的.s4p文件进行去嵌入

- TRL需要许多长且耦合的走线。

工具A给出了错误的结果







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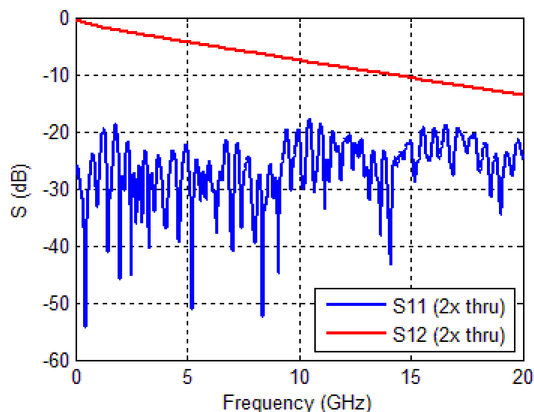
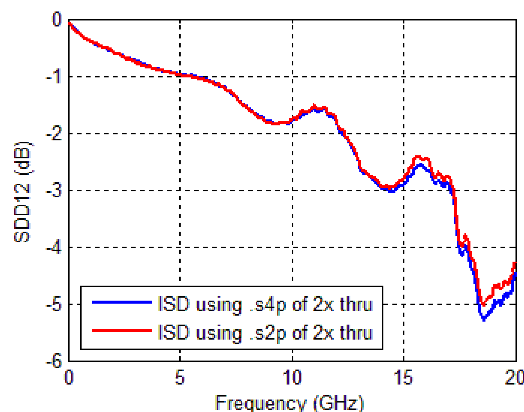
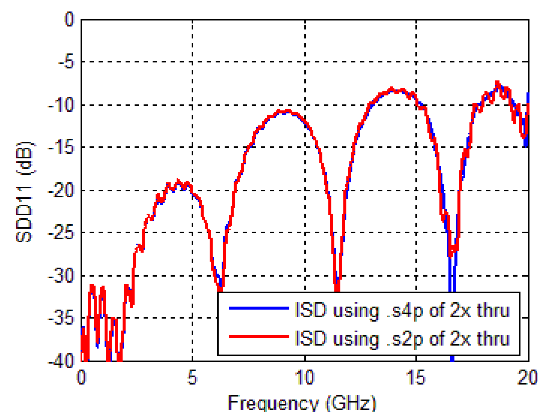
ISD甚至可以使用2xthru的.s2p文件来去嵌入串扰

- And the results are similar!







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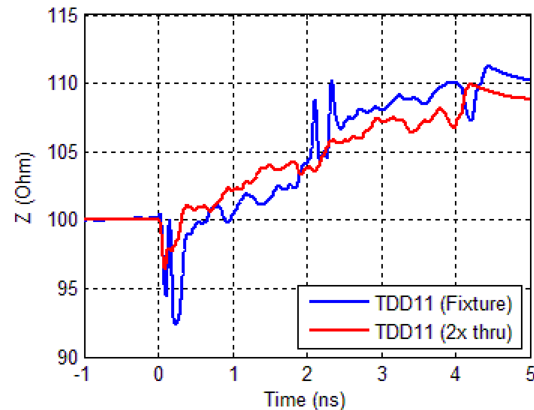
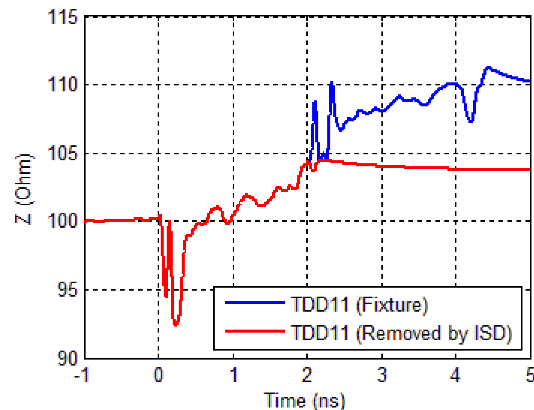
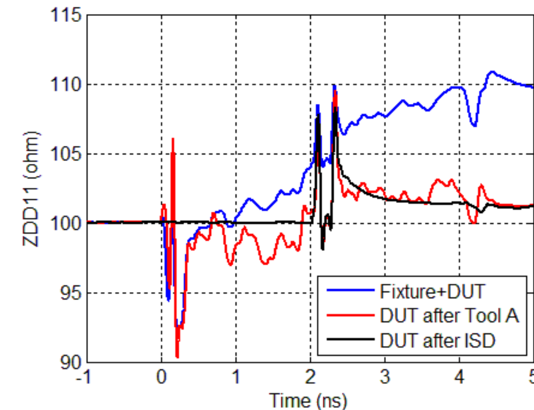
ISD允许大型演示板兼作特征板

- ISD会去嵌入夹具的阻抗，而不管2xthru的阻抗。







Rise time = 40ps (20/80)

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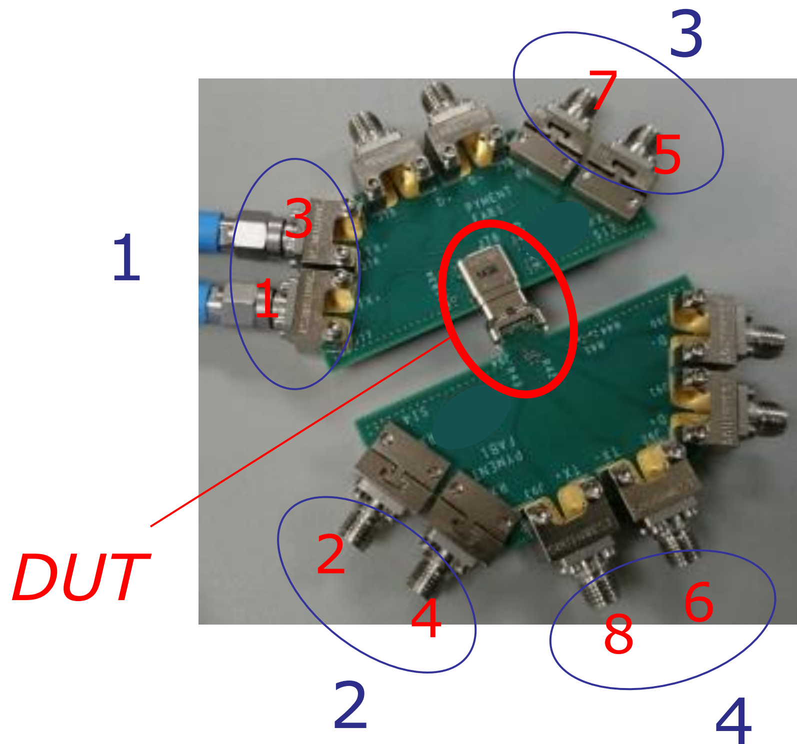
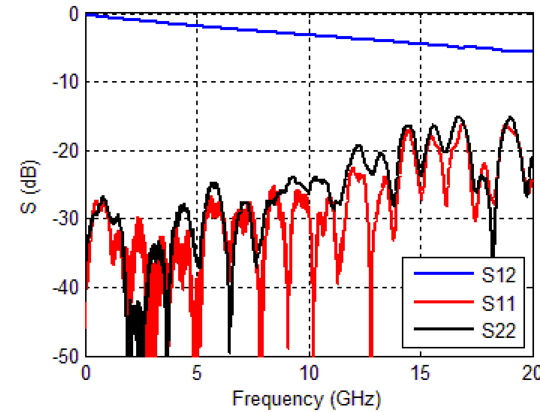
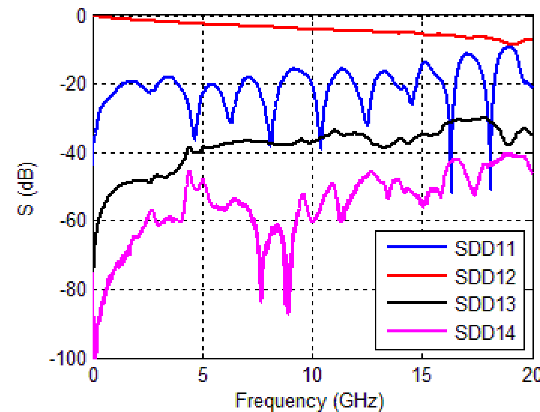
示例3：USB C型连接器性能测试 ISD与工具A

- 良好的去嵌入对于满足合规性规范至关重要





2x thru



Fixture

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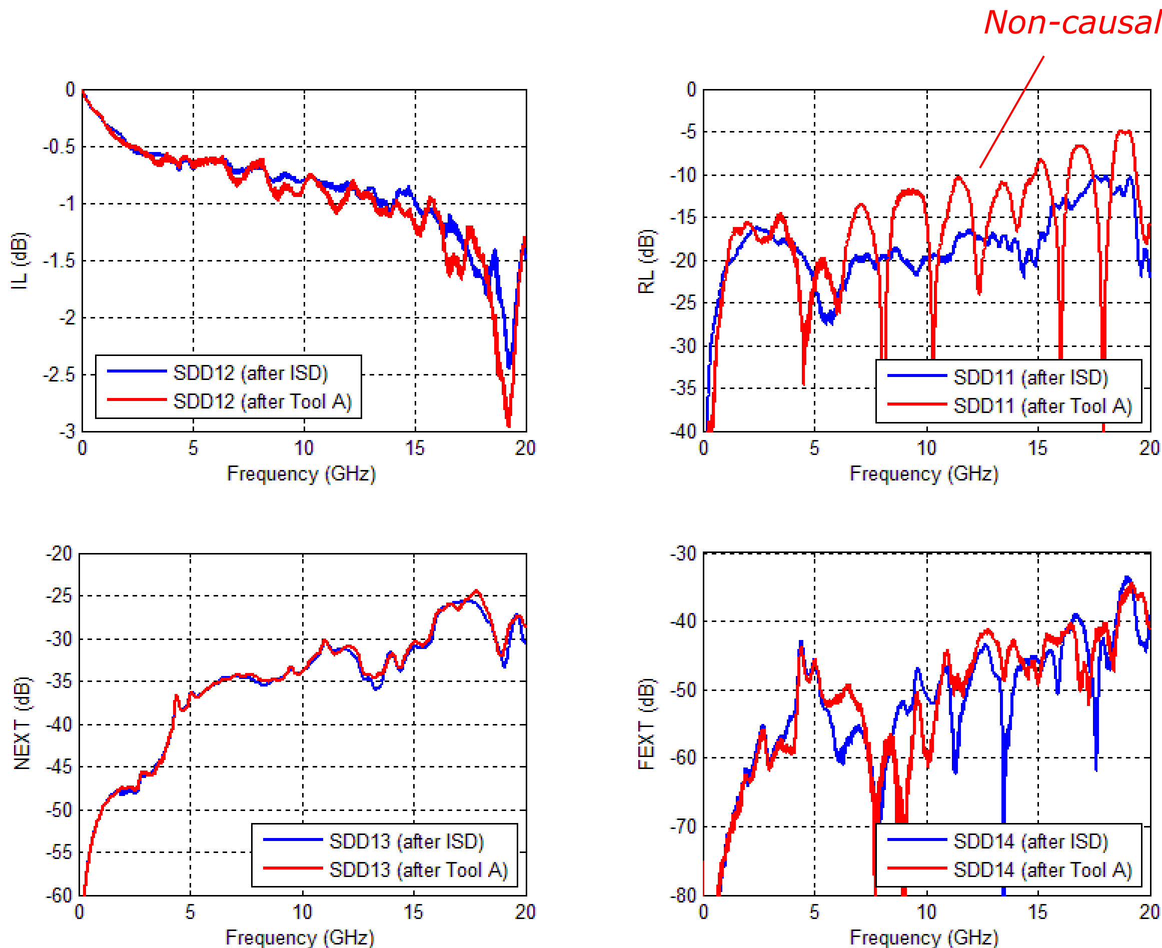
使用ISD和工具A之后的DUT结果哪个更准确?

- Tool A 的结果对于这么小的DUT来说在回损 (RL)上有太多纹波



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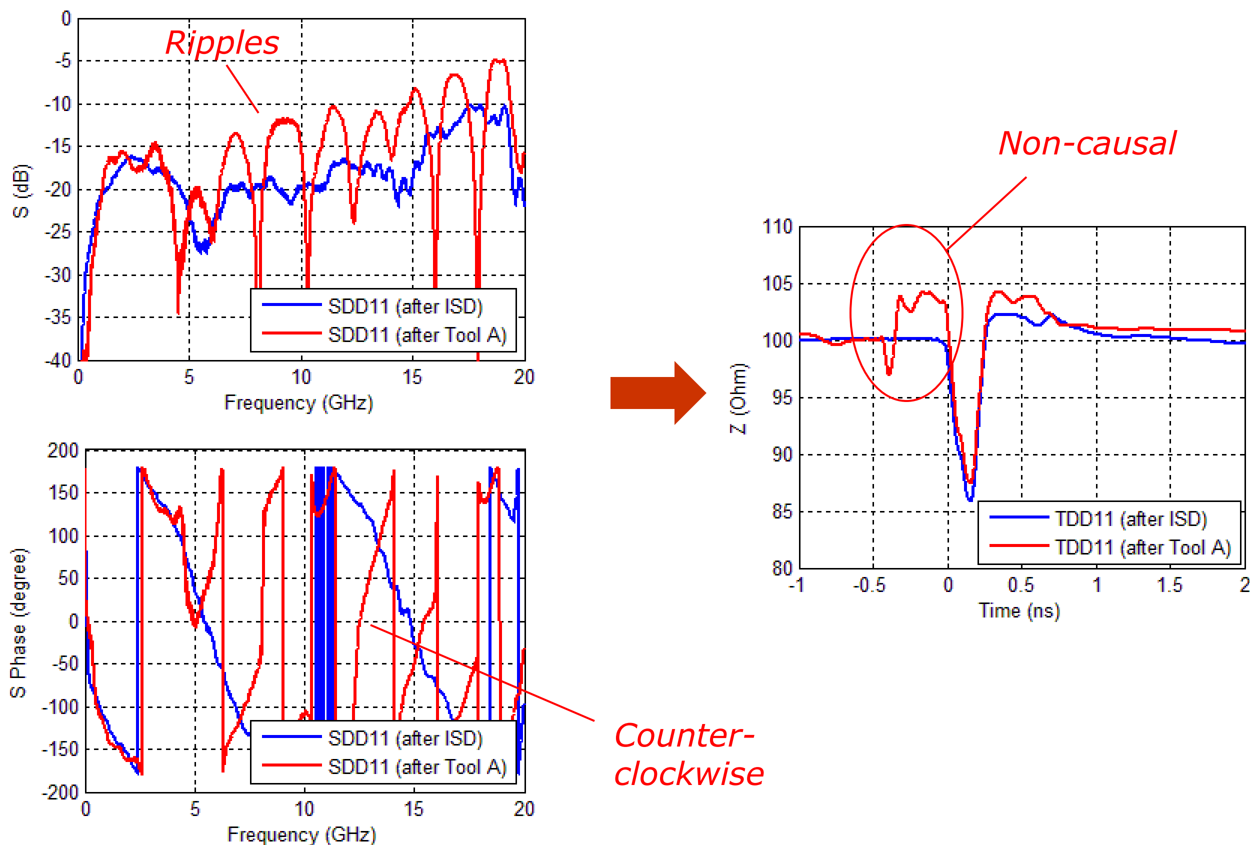
将S参数转换为TDR / TDT显示工具A的结果非因果性

- 逆时针相位角是无因果关系的另一个指标.



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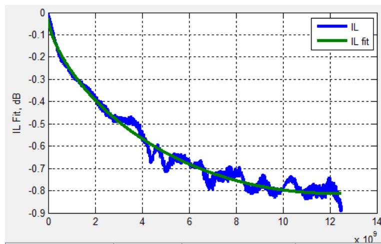
去嵌入会影响合规性规范测试的通过或失败

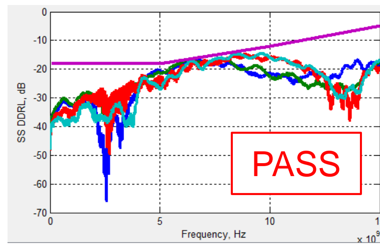
- ISD改进了IMR和IRL（通过合规性工具）

ISD

	Value (Pass/Fail)
ILfit@2.5GHz	-0.4
ILfit@5.0 GHz	-0.6
ILfit@10.0GHz	-0.8
IMR	-45.1
IRL	-23.2
INEXT	-41.5
IFEXT	-49.2
SCD12/SCD21	-23



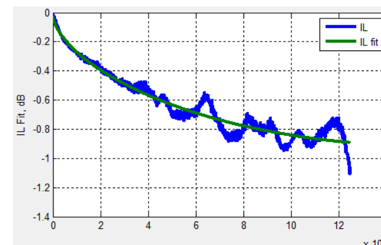
IL



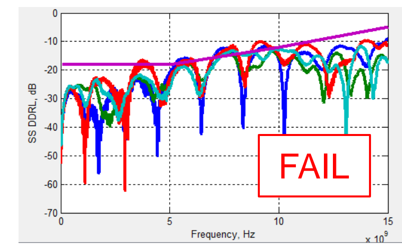
RL

Tool A

	Value (Pass/Fail)	Spec
ILfit@2.5GHz	-0.4	-0.6
ILfit@5.0 GHz	-0.6	-0.8
ILfit@10.0GHz	-0.9	-1.0
IMR	-43.7	-40
IRL	-20.8	-18
INEXT	-41.5	-44
IFEXT	-49.3	-44
SCD12/SCD21	-23.2	



IL



RL

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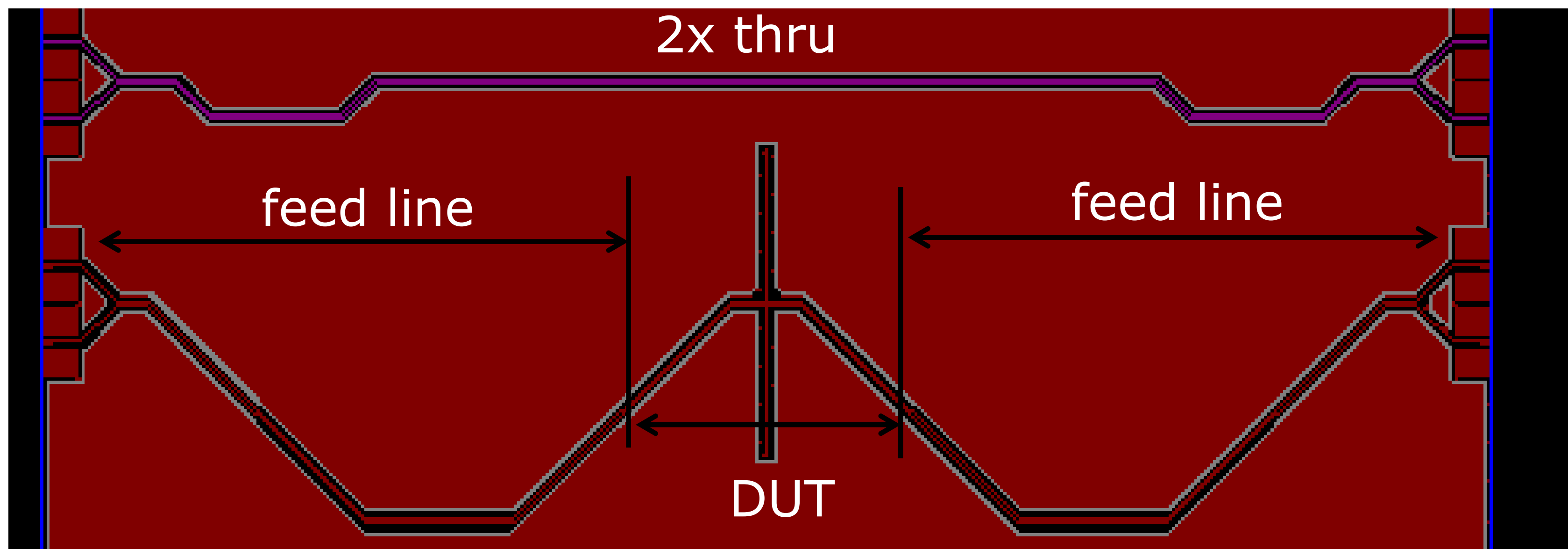
示例4：谐振器
ISD，工具A，仿真之间的比较

- 良好的去嵌入对于设计验证（即相关性）和改进至关重要。



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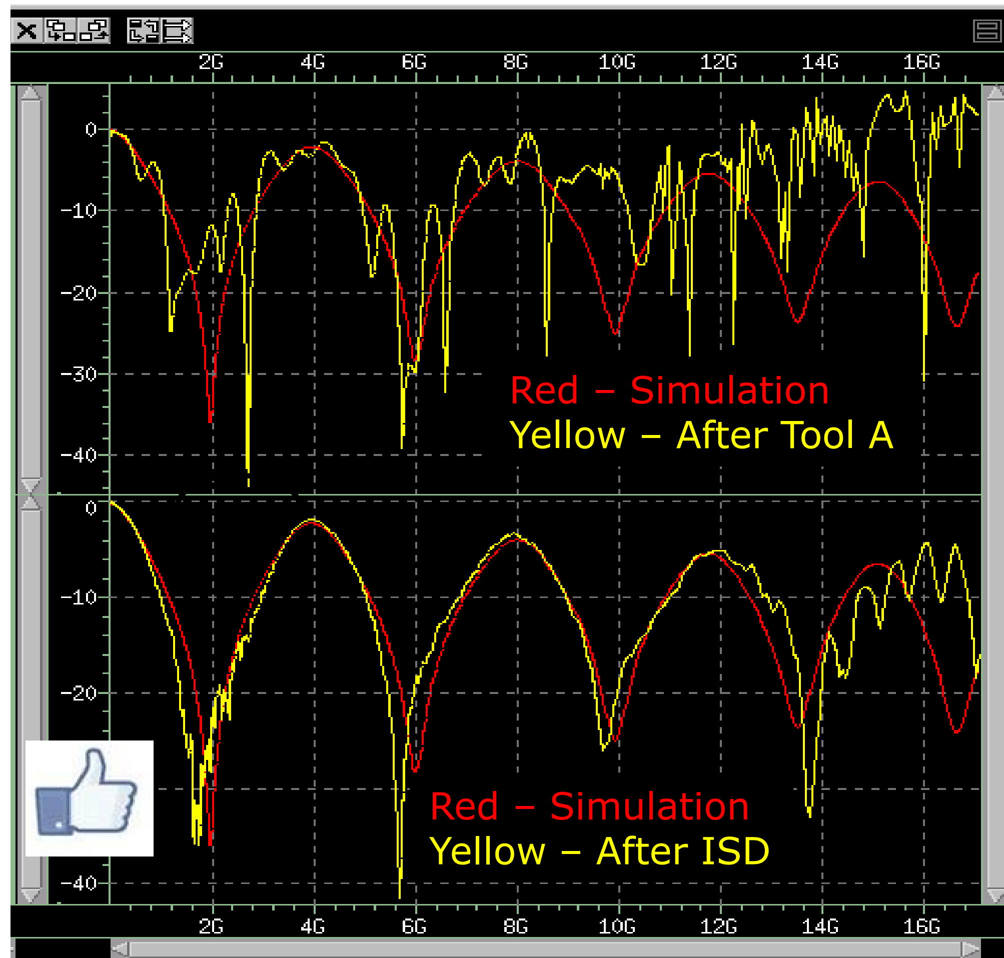
SDD11
ISD与仿真的相关性



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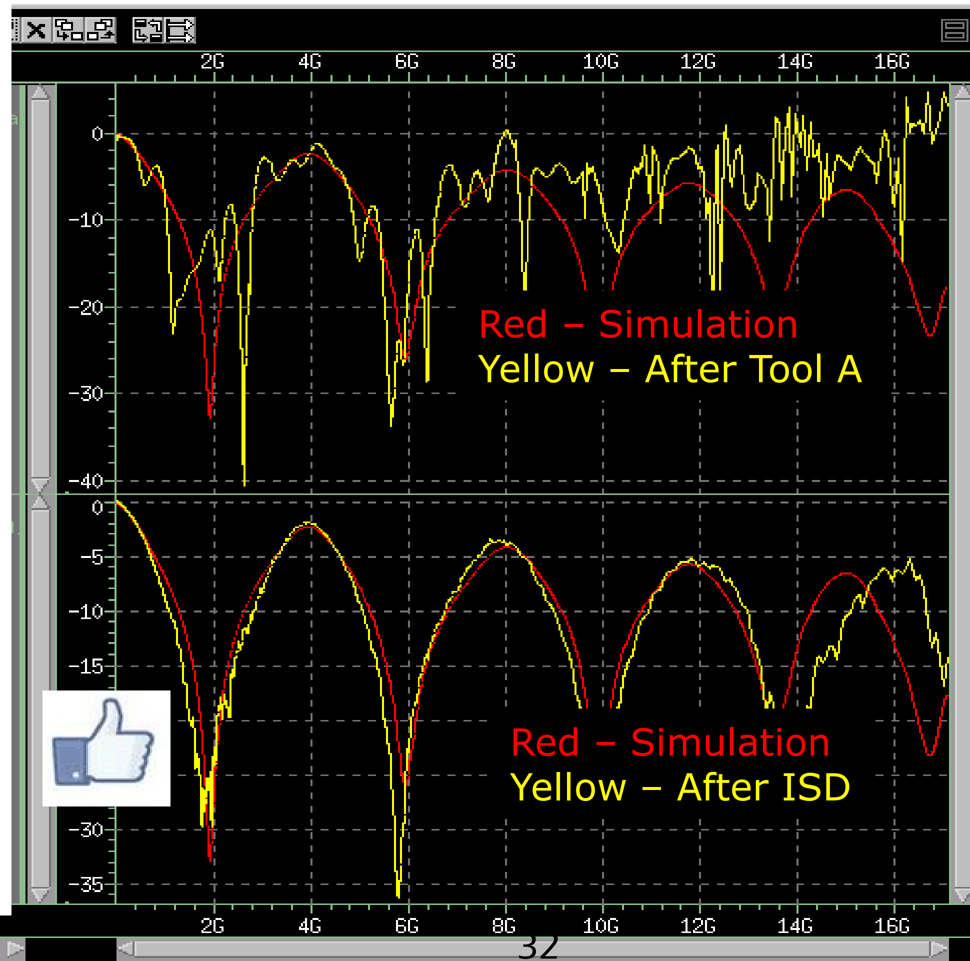
SCC11
ISD与仿真的相关性

- 良好的相关性对于改进设计至关重要。



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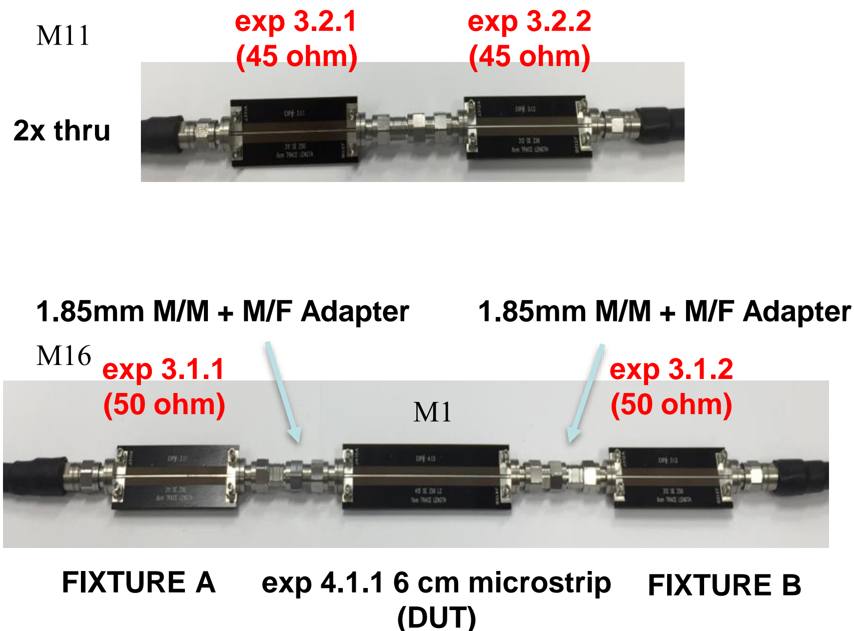
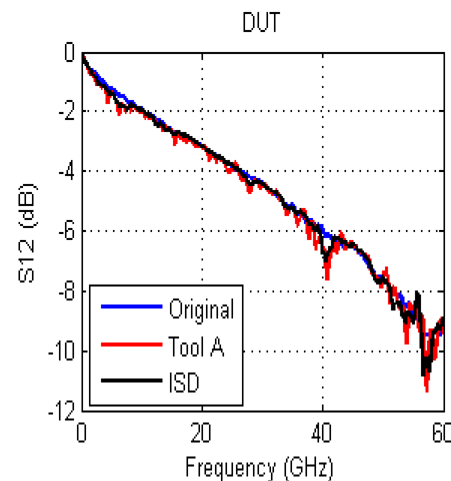
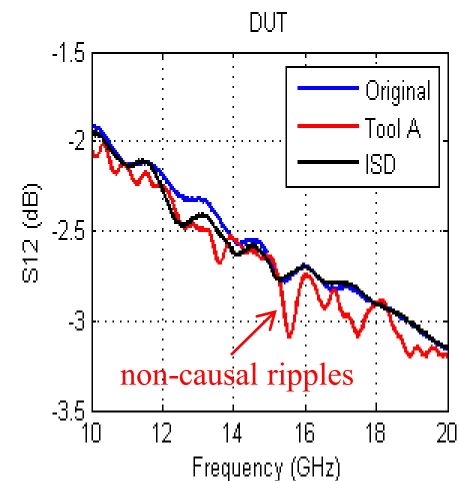
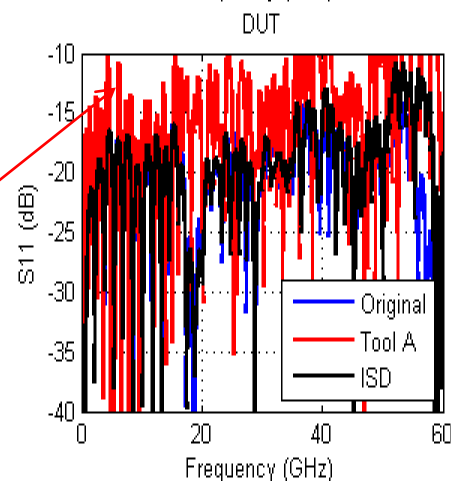
示例5：IEEE P370即插即用套件使用45欧姆2XThru去嵌入50欧姆夹具*

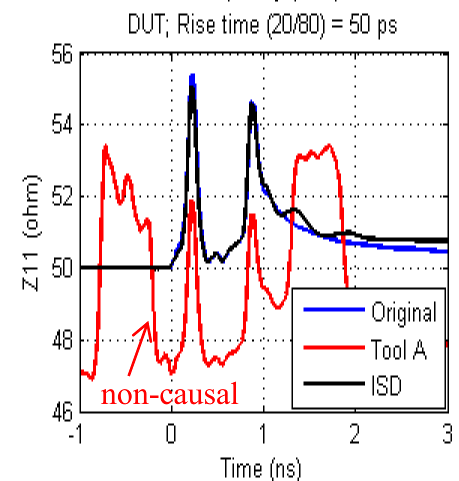
*模拟可能的PCB阻抗变化











不正确的RL不适合DK / DF / SR提取。

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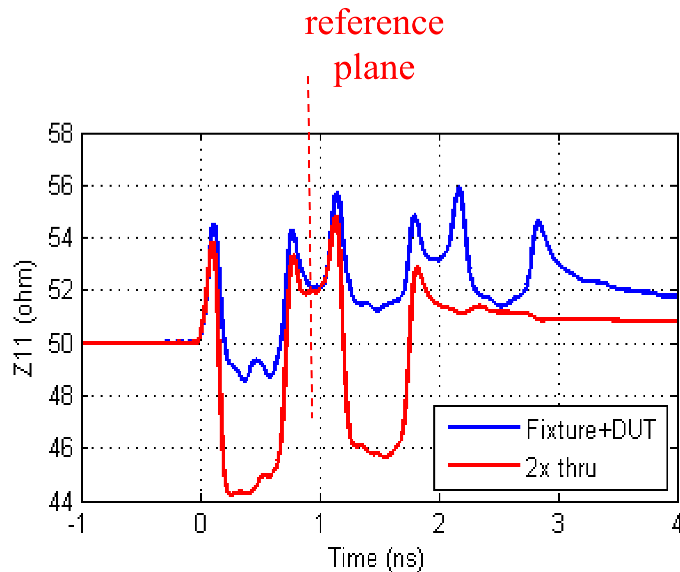
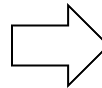
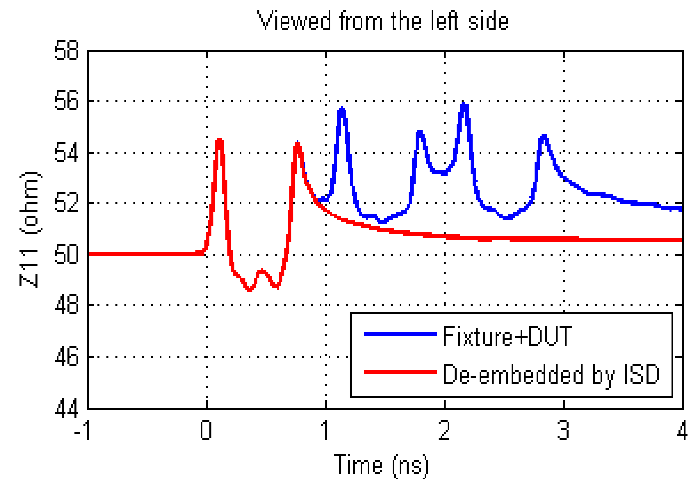
2x thru vs. 夹具阻抗

- ISD 去嵌入夹具阻抗, 不是 2x thru的阻抗.







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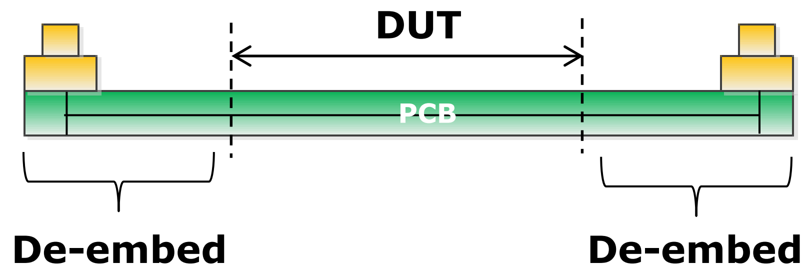
示例6: PCB 走线衰减

ISD vs. eigenvalue (Delta-L)

- 从长走线中去嵌入短走线得到走线的衰减.

$$L_{DUT} = L_{LONG} - L_{SHORT}$$



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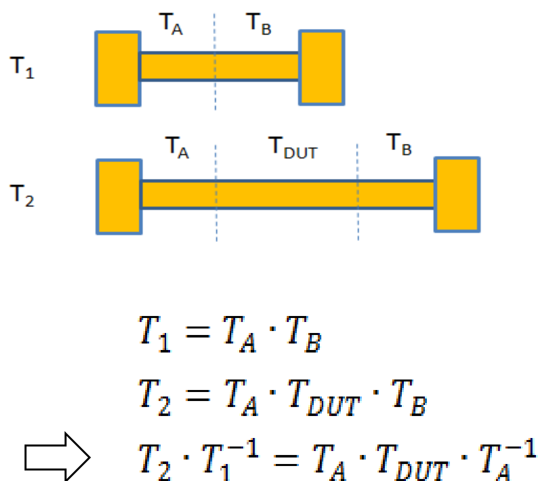
特征值解决方案：不去嵌入仅用于计算走线衰减

- 将S转换为T以获取短和长的走线结构
- 假设短走线和长走线结构的左侧和右侧相同
- 假设DUT是统一的传输线
- 仅跟踪衰减被写在一个公式中



For uniform transmission line:

$$T_{DUT} = P \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{pmatrix} \cdot P^{-1}$$

Let $T_2 \cdot T_1^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix}$

$$\Rightarrow e^{-\gamma l} = \frac{(a+d) \pm \sqrt{(a-d)^2 + 4bc}}{2}$$

eigenvalue

modal propagation constant

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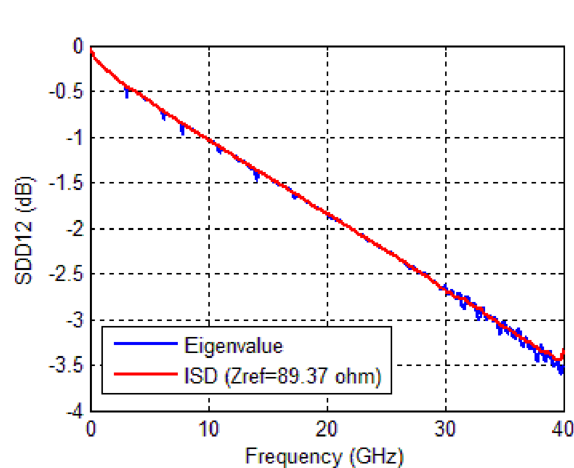
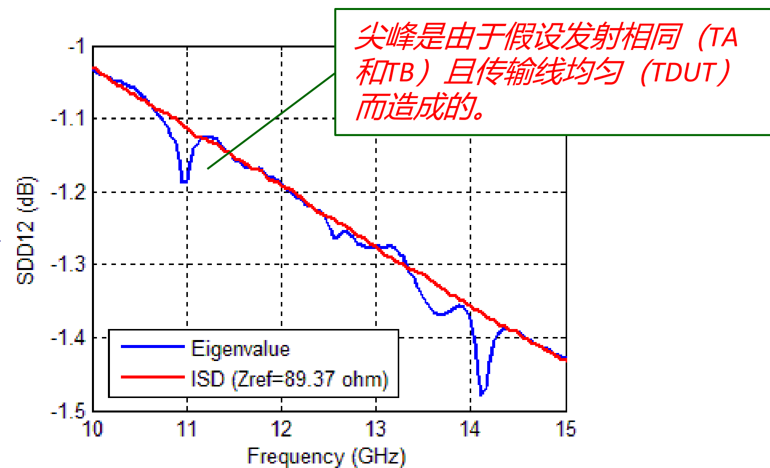
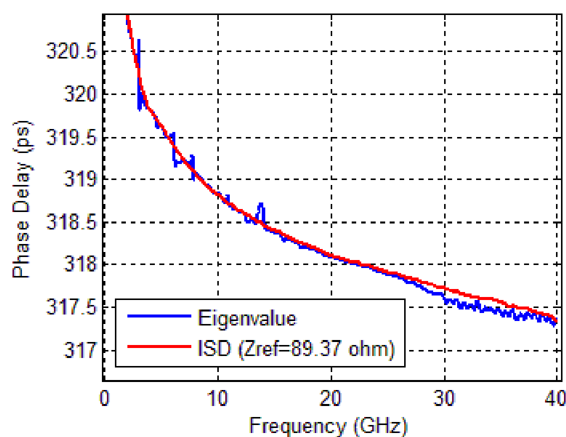
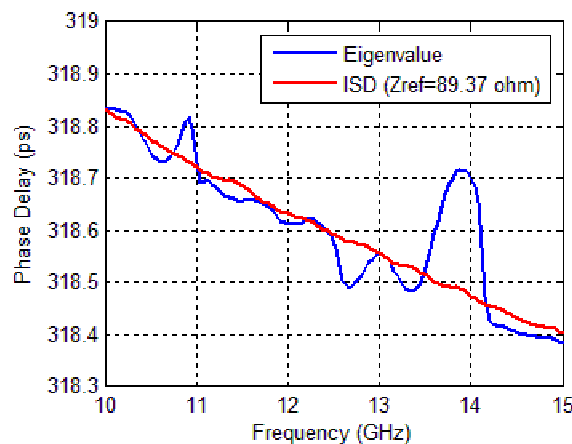
情况1：2”（= 7” -5”）走线衰减特征值解决方案容易出现尖峰









ISD的无尖峰结果有助于以后提取DK和DF

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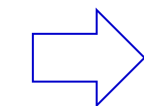
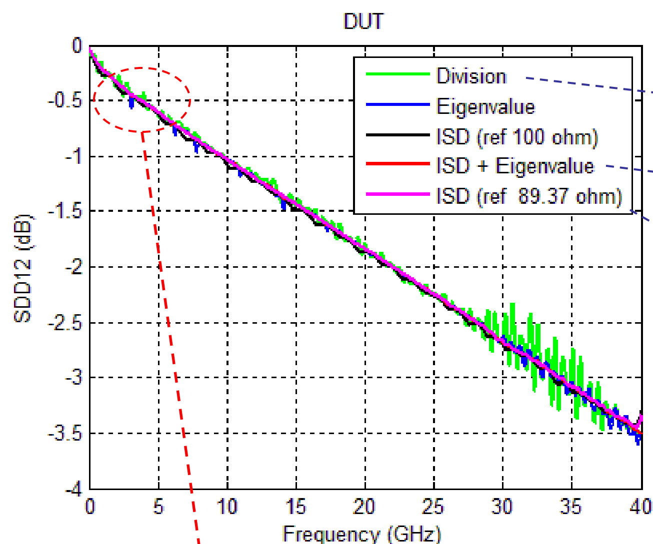
一键即可将ISD与特征值进行比较，还有更多…

Run Help

- Split 2x Thru only
- Extract DUT
- Batch mode
- Eigenvalue (Delta-L) method
- Compare ISD with Eigenvalue
- Renormalize and deskew DUT
- Material Property Extraction (MPX)



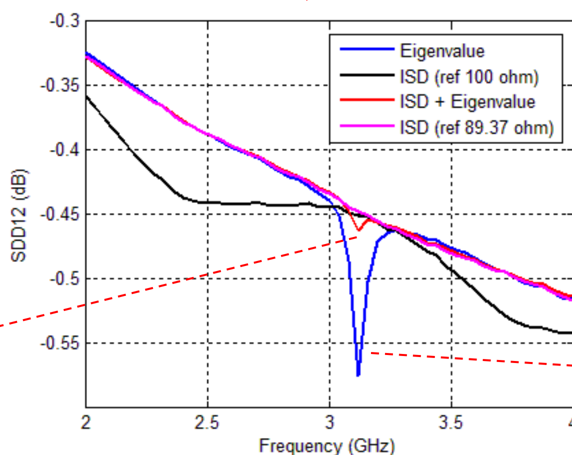
One click does it all



直接dB减法

ISD结果的特征值

重新标准化ISD结果通过走线阻抗（自动计算



尖峰是由于相同发射（TA和TB）和统一传输线（TDUT）

尖峰是由于假设TA和TB相同和统一传输线（TDUT）

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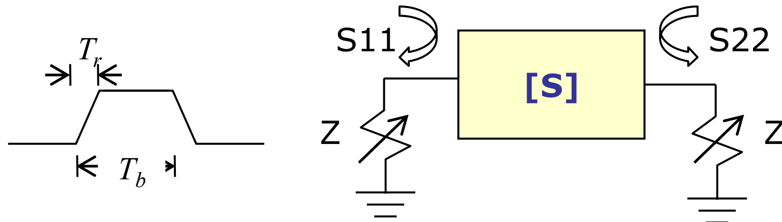
如何定义走线阻抗
PCB走线是不均匀的传输线

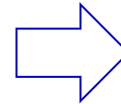
- 通过最小的RL定义阻抗*

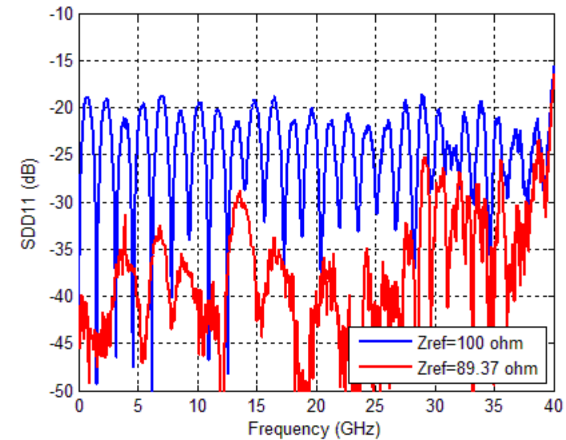


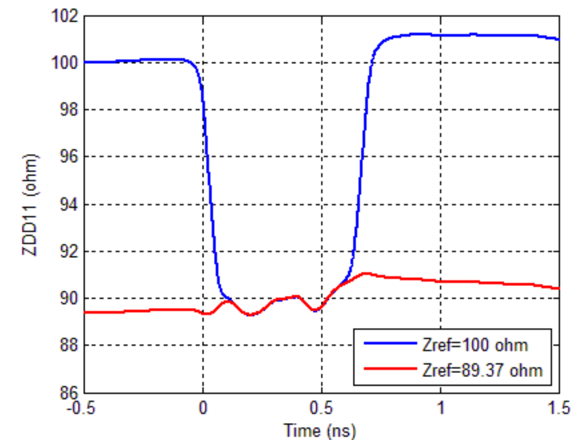
Minimize:

$$\varphi = \int_{f_{\min}}^{f_{\max}} \left\{ \left|S_{11}(f)\right|^2 + \left|S_{22}(f)\right|^2 \right\} \cdot \left|w(f)\right|^2 df$$

$$w(f) = \frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}$$







* J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, "Aristotle: A fully automated SI platform for PCB material characterization," DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.

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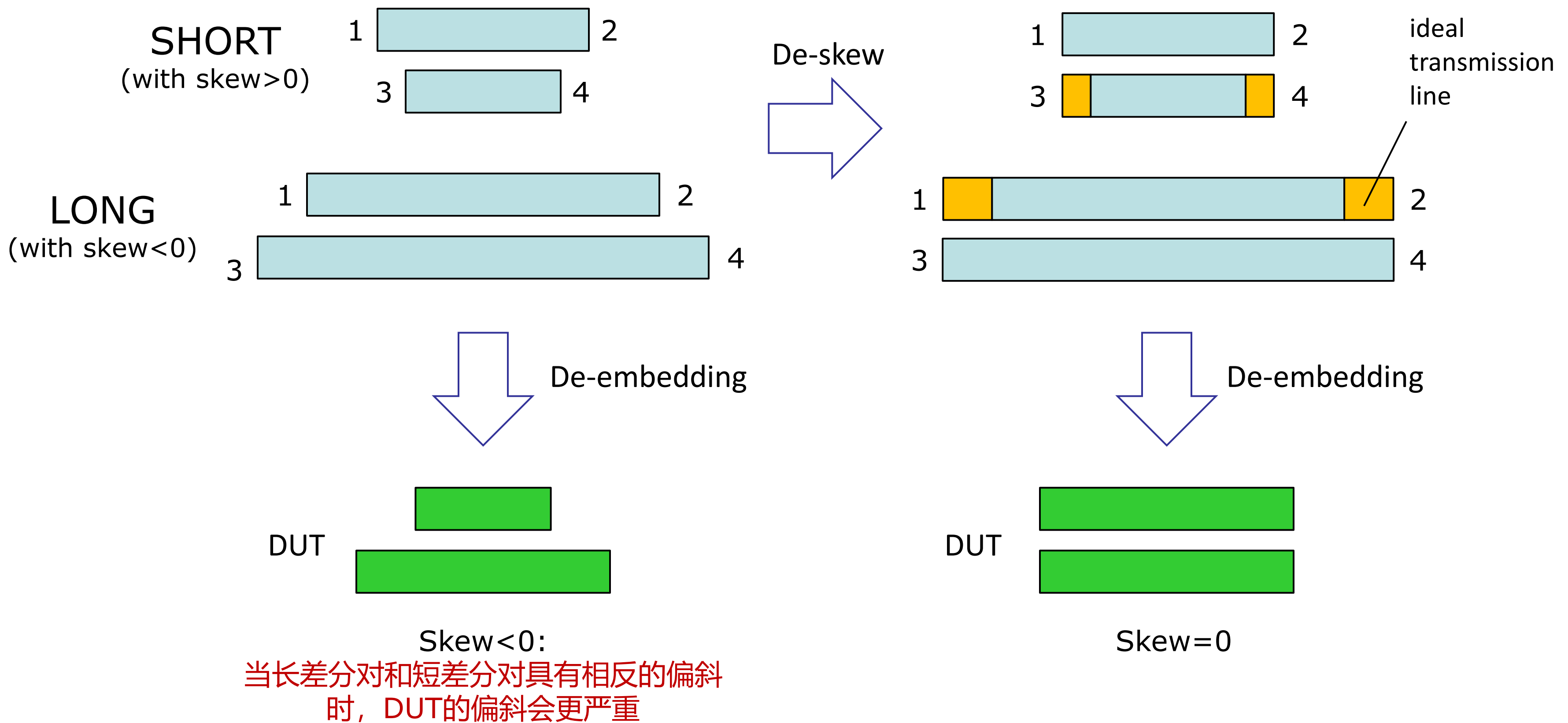
时间偏斜去嵌入

- 理想的传输线到偏斜去嵌入



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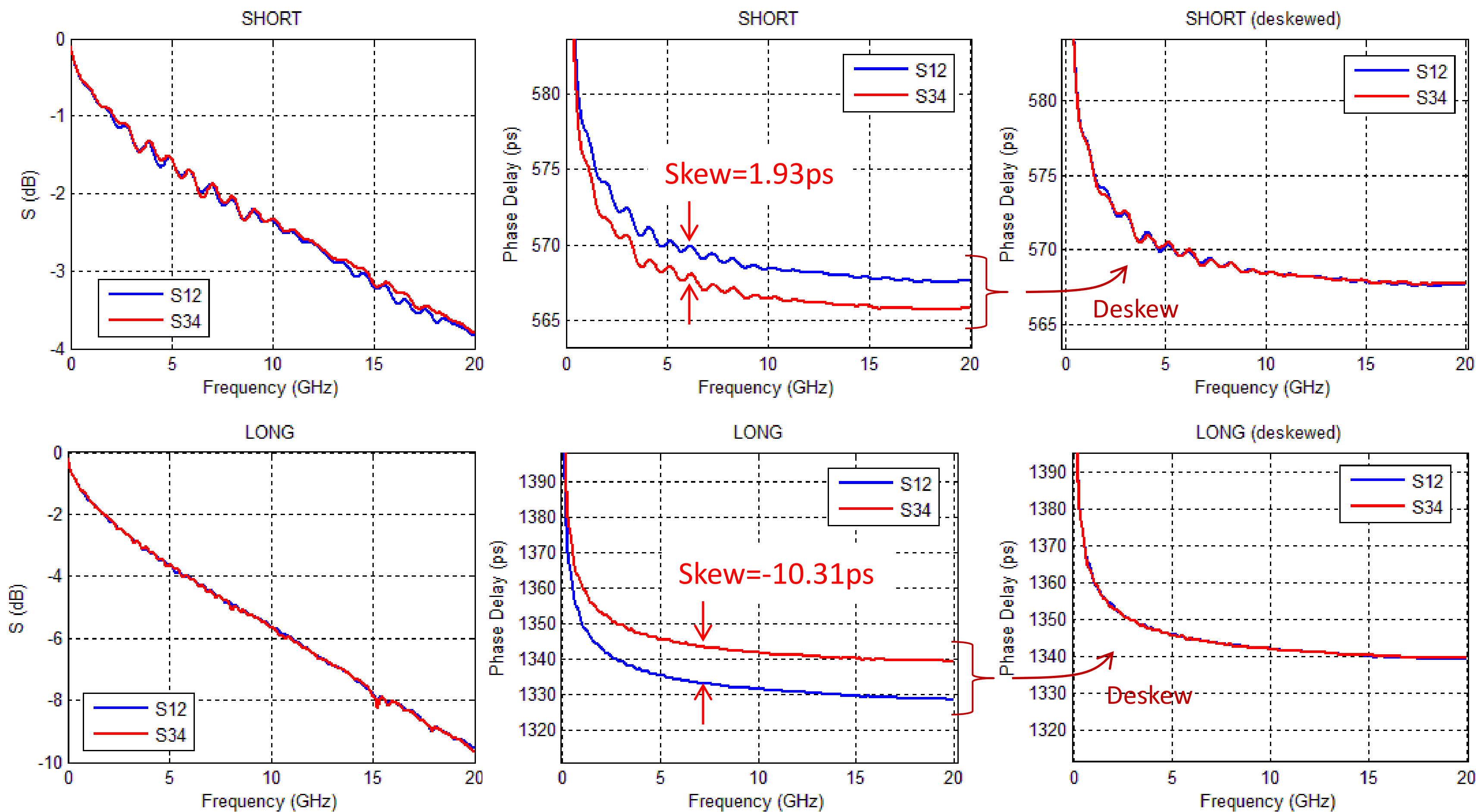
ISD可选地自动对原始数据进行时间偏移校正



LONG=8”
SHORT=3”

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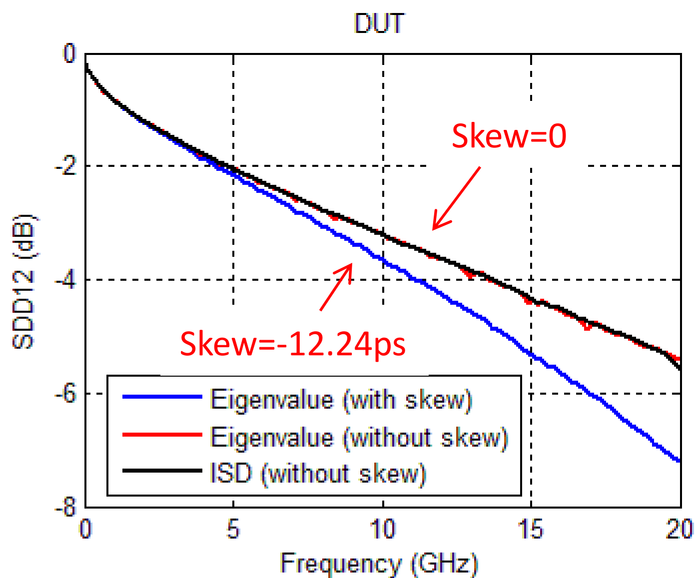
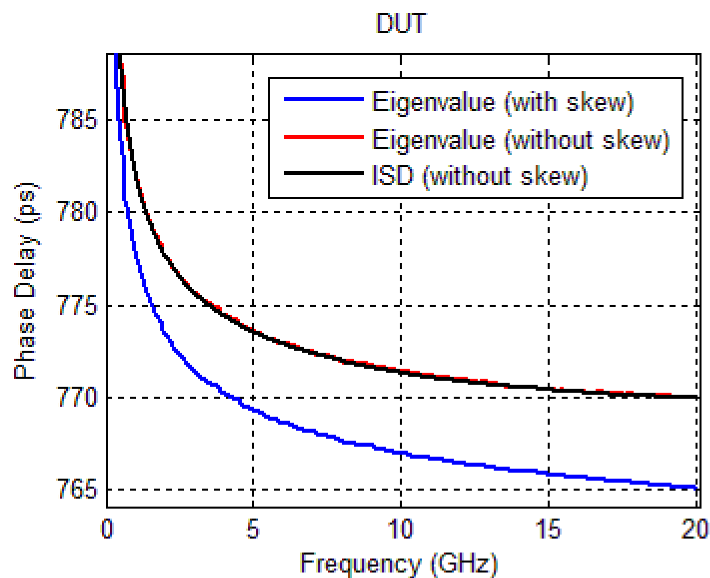
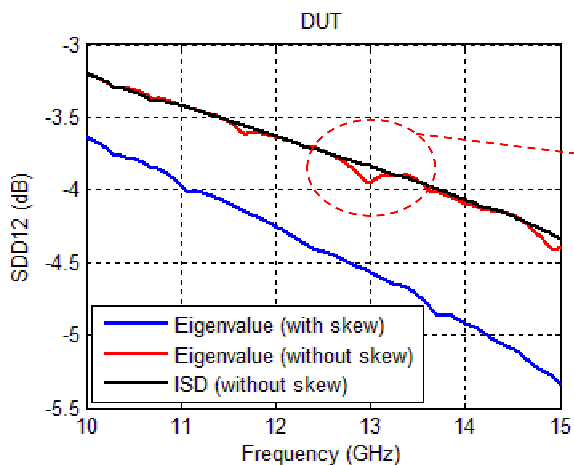
情况2：无论有无时间差，提取的走线衰减都可能非常不同







特征值解决方案在一个有趣的频率（大约12.9 GHz）上有一个下降

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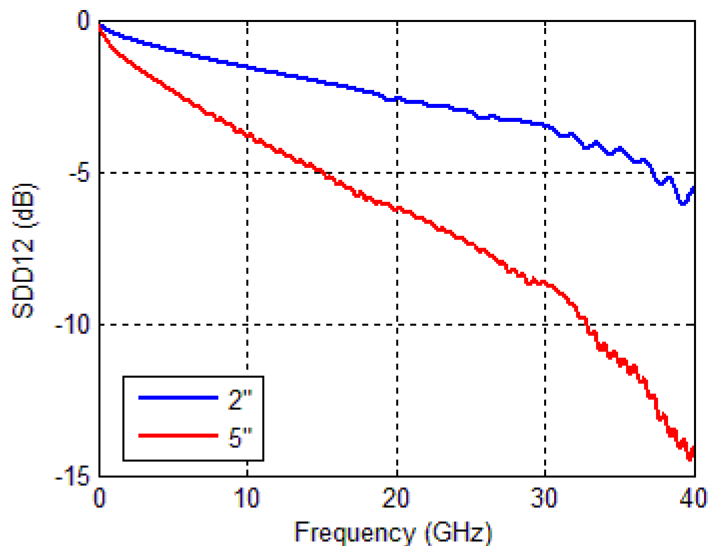
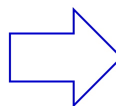
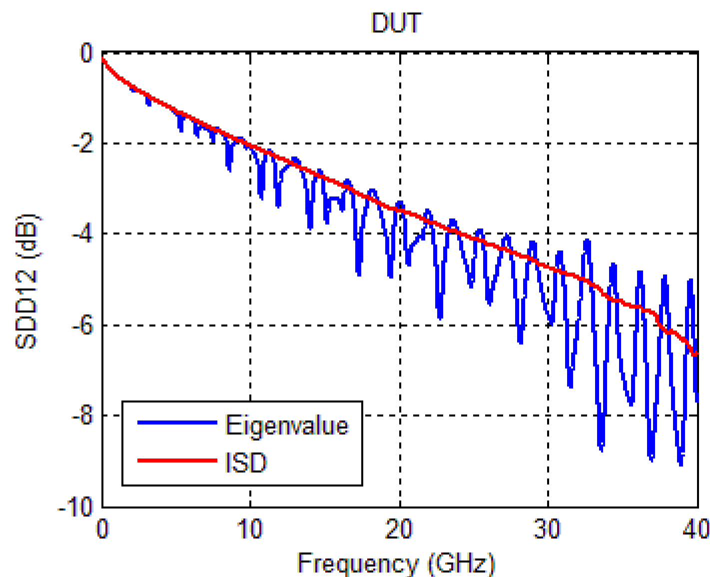
情况3：在这种情况下，特征值（Delta-L）解变得不稳定，但是为什么呢?







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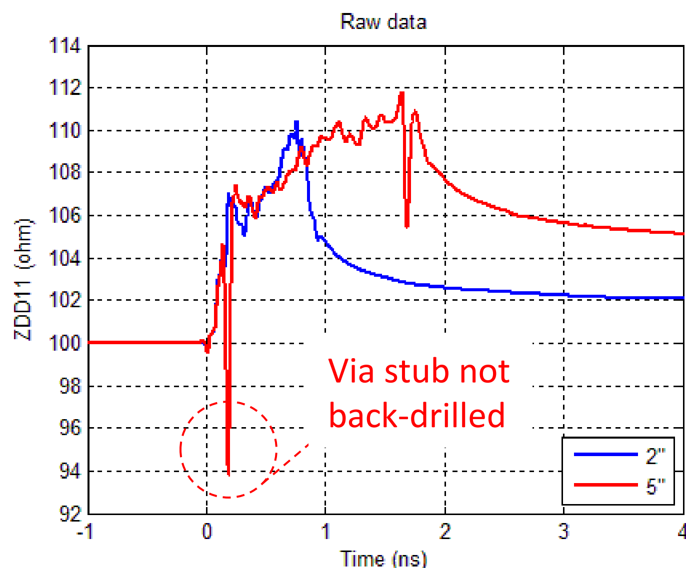
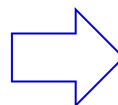
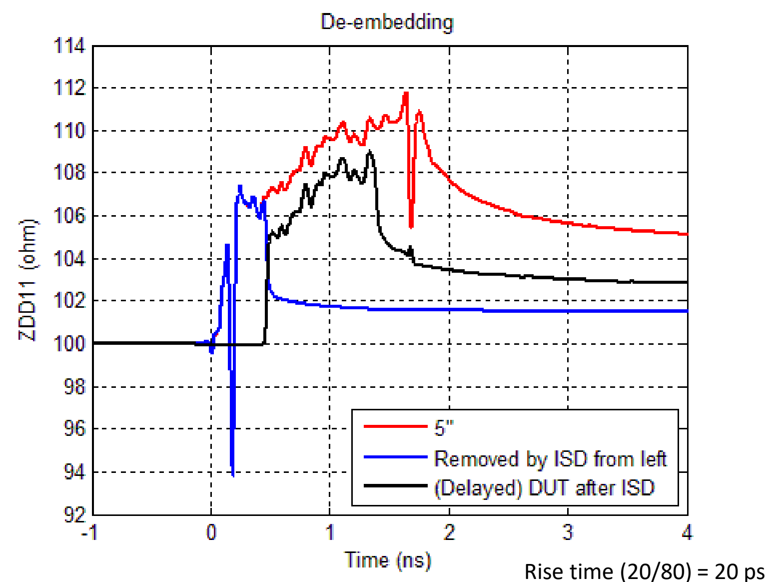
TDR of raw data reveals why…
2" structure was back-drilled but 5" was not

- Eigenvalue solution assumes 2" and 5" structures have identical launches.
- ISD de-embeds 5" structure's launch correctly.







Rise time (20/80) = 20 ps

ISD saves $$$ and time for not spinning another board.

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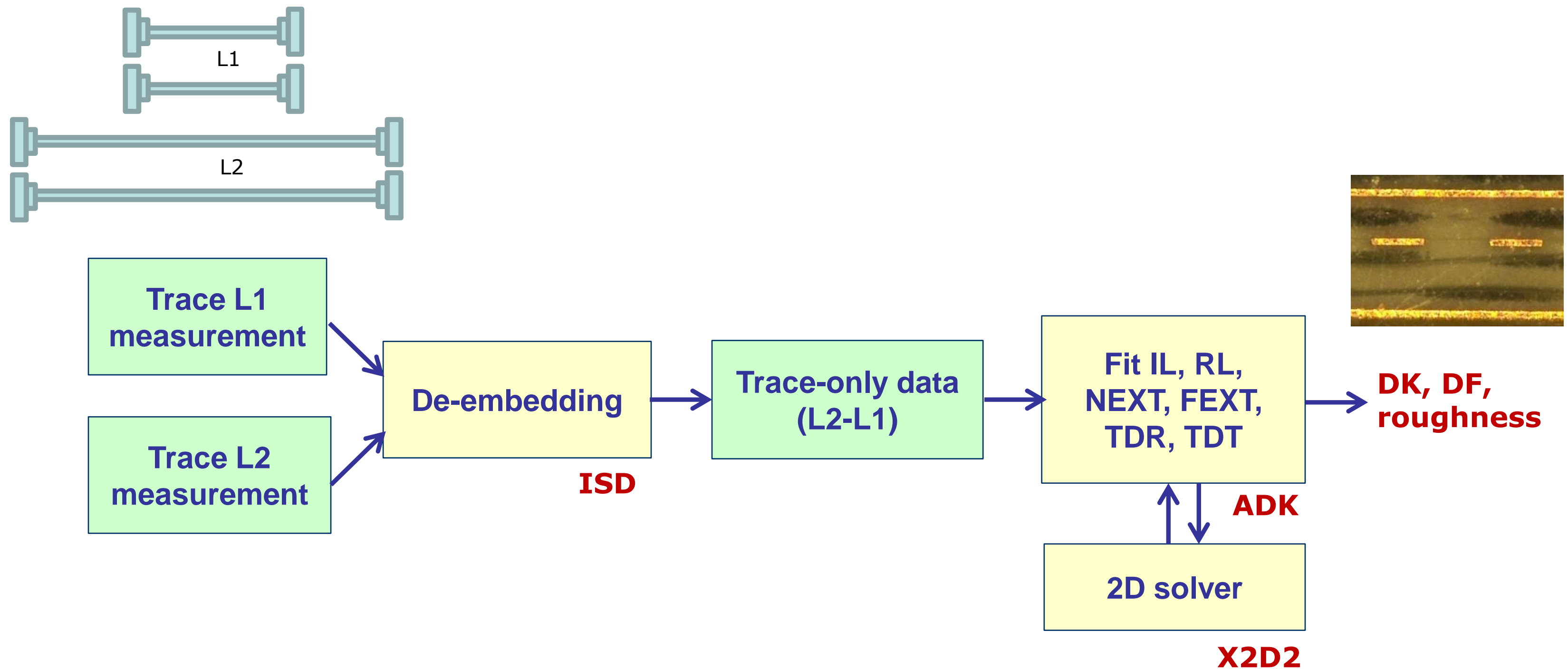
示例7：材料属性提取DK，DF和粗糙度

- 仅通过匹配去嵌入的走线数据的所有IL，RL，NEXT，FEXT和TDR / TDT的自一致方法来提取DK，DF和粗糙度



Automated extraction flow

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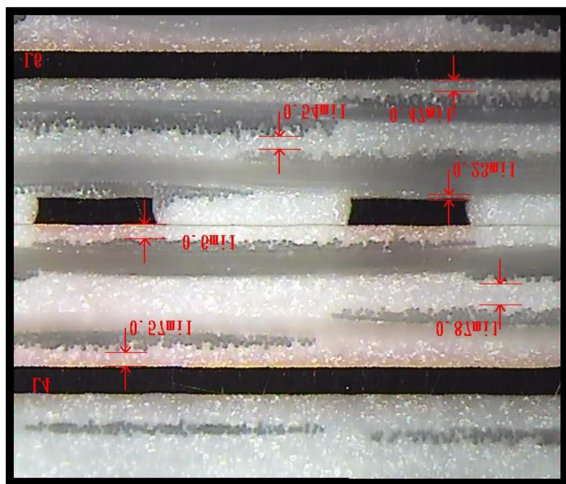
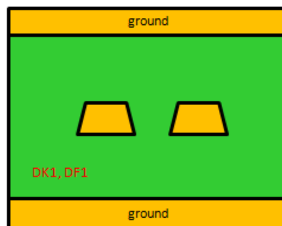
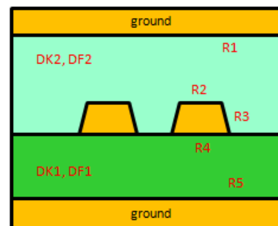
横截面模型

优化变量：
DK1，DF1，DK2，DF2
R1，R2，R3，R4，R5（粗糙度）
金属宽度和间距

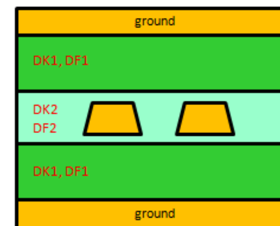




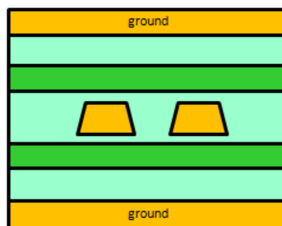
Model 1



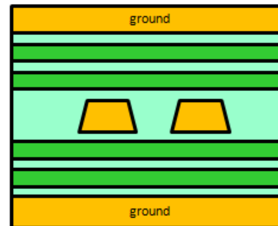
Model 2



Model 3



Model 4



Model 5

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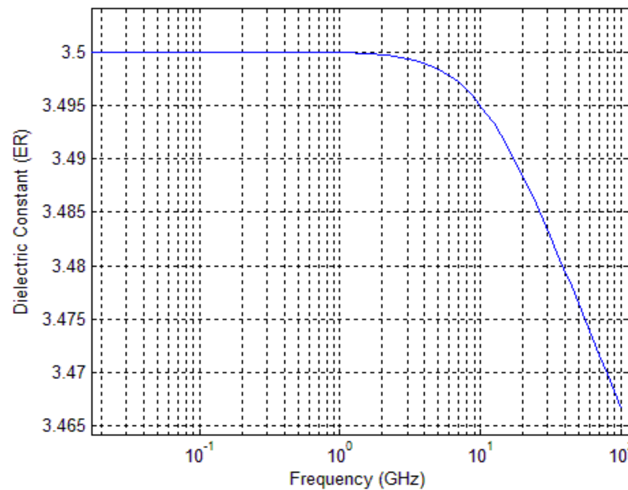
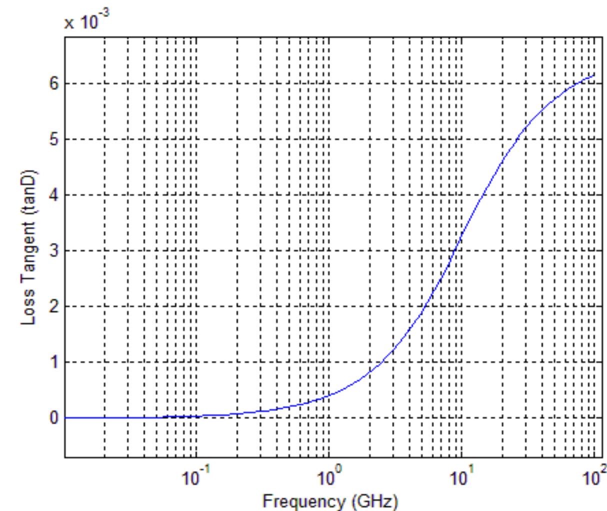
因果介电模型

- 宽带德拜（或Djordjevic-Sarkar）模型
- 只需要4个变量：　ε_∞ , $\Delta\varepsilon$, m_1 , m_2

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$

$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$





$\varepsilon_\infty = 3.35$, $\Delta\varepsilon = 0.15$, $m_1 = 10$, $m_2 = 14.5$

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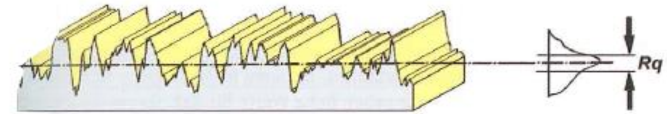
表面粗糙度模型

- 有效电导率（由G. Gold和K. Helmreich在DesignCon 2014上发表）仅需两个变量：σ_{bulk} ，R_q

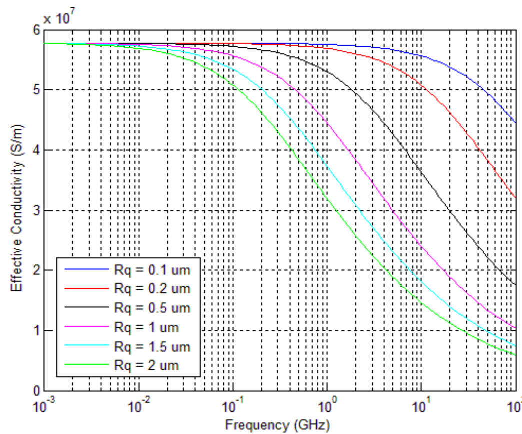
Parameter	Description	Standard
R_q	root mean square	DIN EN ISO 4287
R_a	arithmetic average	DIN EN ISO 4287, ANSI B 46.1
R_k	core roughness depth	DIN EN ISO 13565
R_z	average surface roughness	DIN EN ISO 4287

Table 1: *Statistical parameters to describe surface roughness*

$$\sigma(x)=\sigma_{bulk}\cdot CDF(x)=\sigma_{bulk}\cdot\int_{-\infty}^{x}PDF(x)du=\sigma_{bulk}\cdot\int_{-\infty}^{x}e^{-\frac{u^2}{2R_q^2}}du$$



- 在数值上求解 $\nabla^2\overline{B}-j\omega\mu\sigma\overline{B}+\frac{\nabla\sigma}{\sigma}\times\left(\nabla\times\overline{B}\right)=0$ 和使功率等于光滑表面的功率 σ_{eff}



$\sigma_{bulk}=5.8\times10^7$ s/m

- ❖ 简单
- ❖ 与场求解器一起很好地工作给出粗糙度对所有IL，RL，NEXT和FEXT的影响

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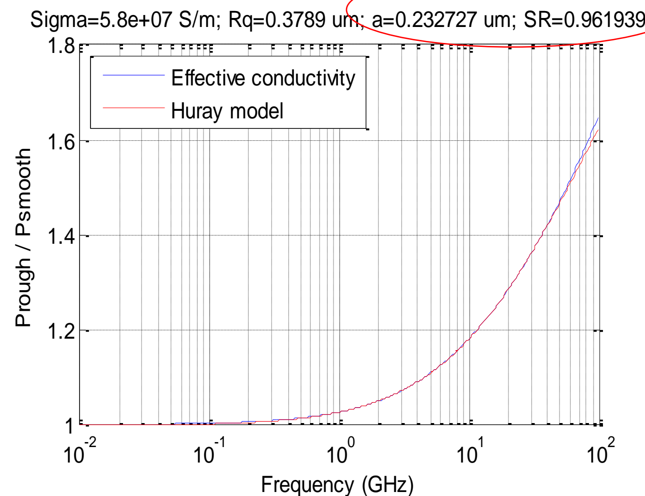
将有效电导率转换为Huray模型

- Huray model

$$\frac{P_{rough}}{P_{smooth}} \approx 1 + \frac{3}{2} \cdot SR \cdot \left(\frac{1}{1 + \frac{\delta(f)}{a} + \frac{1}{2}\left(\frac{\delta(f)}{a}\right)^2} \right)$$

$$\delta(f) = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad ; \quad a = \text{radius} \quad ; \quad SR = \text{surface ratio}$$

- Curvefit* P_{rough} / P_{smooth} to convert σ_{bulk} , R_q to a , SR



*Automated in ADK

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DK/DF/SR 提取 (from ADK)

Extract DK, DF and Roughness

Tools

Extract DK, DF and Roughness

- Trace only
- Delta L

Touchstone File (Trace only)

Browse ... D:\MPX_L7_T5_WS1_Z90_T1234.s4p_DUT.s4p

Stripline (Three layers)

Length = 2 inch

From 0 to 100 GHz

Top Ground Plane / DK / td4 / DK2 / tm / wt / wb / td3 / td2 / DK / pitch / td1 / Bottom Ground Plane

Create new Touchstone file

Length	2	inch
Minimum Frequency	0	GHz
Maximum Frequency	40	GHz
Number of Points	801	

Linear / Log

Reference Impedance 50 Ohm

Simulate Only

Cross section (in mil)

td1	4.65	td2	1.19
td3	2.38	td4	3.85
tm	1.21	pitch	14.971
wt	5.504	wb	5.799

Fixed: Thickness / Width / All

DK & DF at 1 GHz

DK	3.439	DF	0.004123
DK2	3.628	DF2	0.000664

Fixed M1= 7.840! M2= 16.98

Roughness (Rq)

Top ground	0.3103	um
Signal	0.3103 0.3	um
Bottom ground	0.3103	um
Sigma	5.8e7	S/m

Fixed Rq

* Optimized

Auto de-skew

Run

Multiple templates

Updated after extraction

Different roughness for each surface

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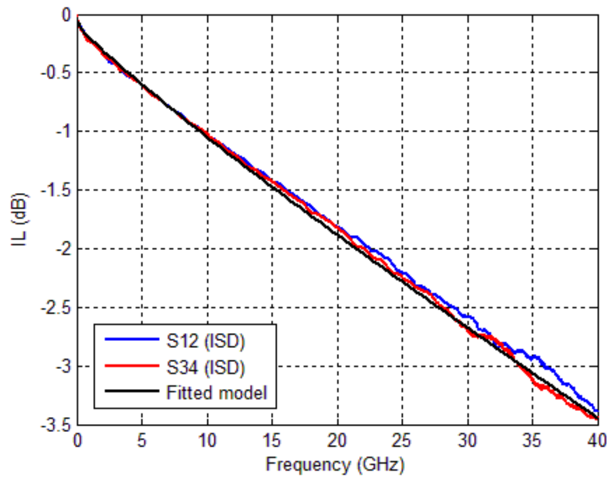
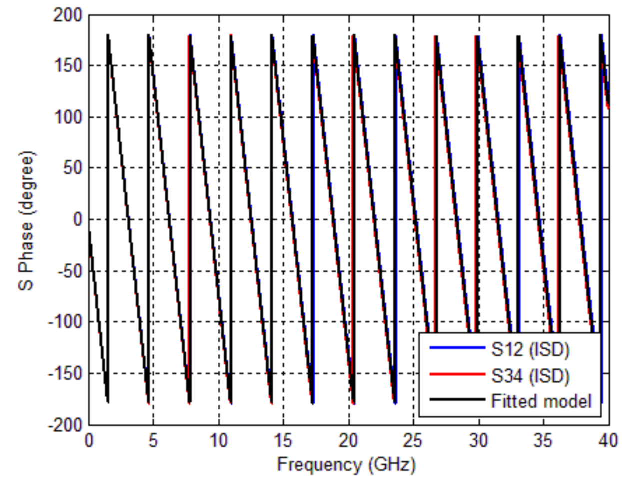
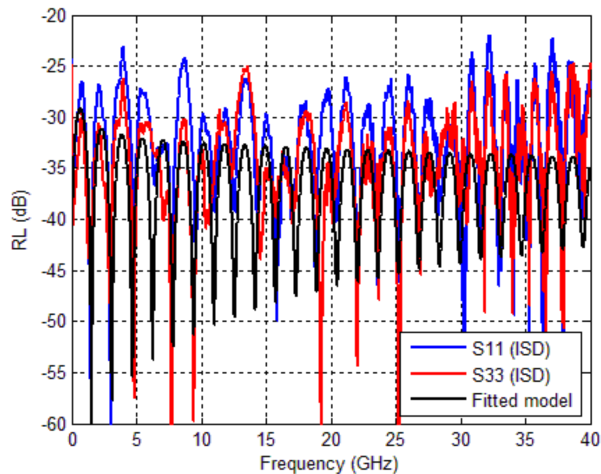
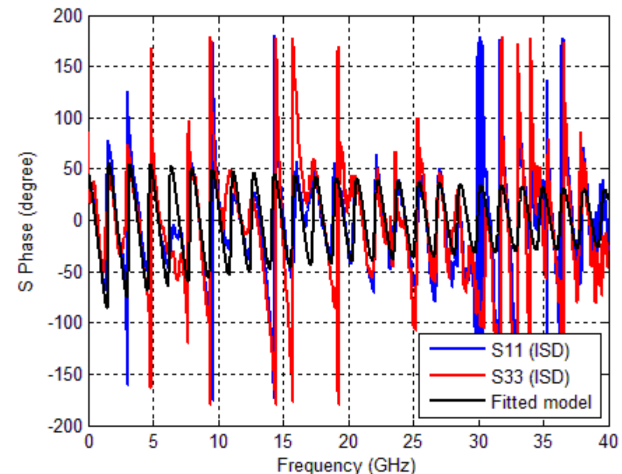
IL and RL匹配









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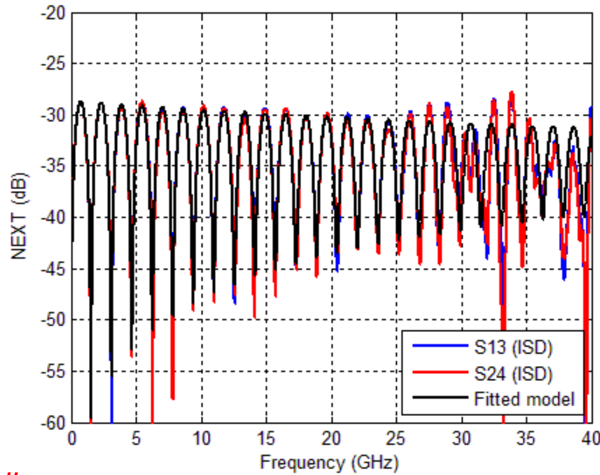
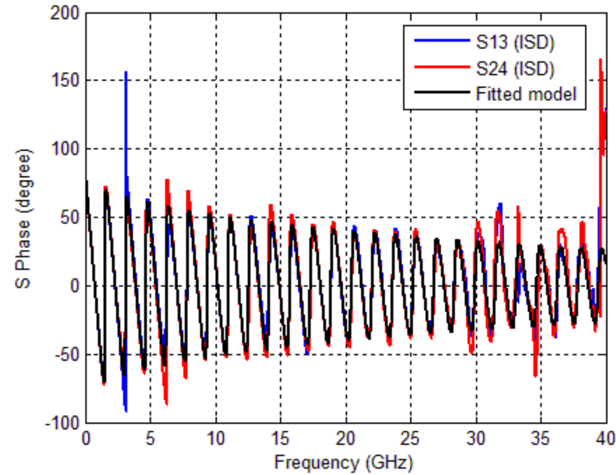
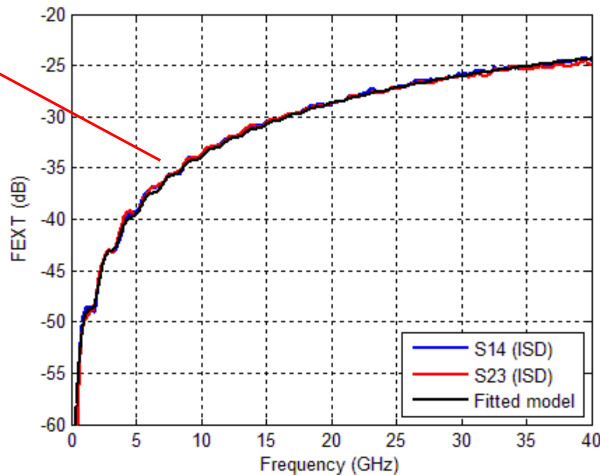
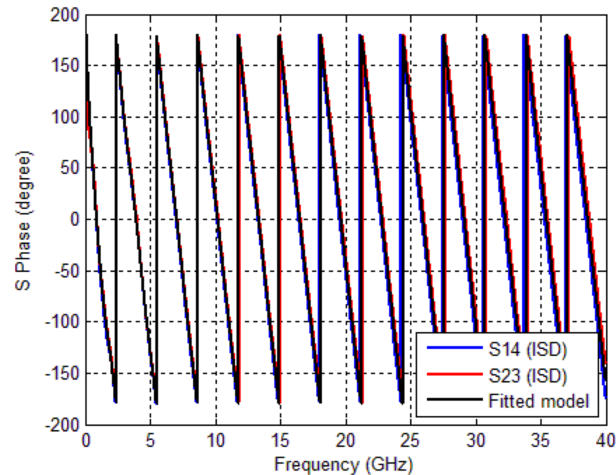
NEXT and FEXT匹配





Large FEXT implies inhomogeneous dielectric





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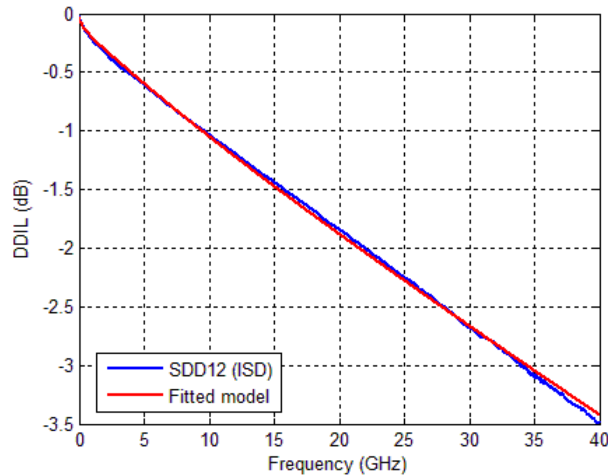
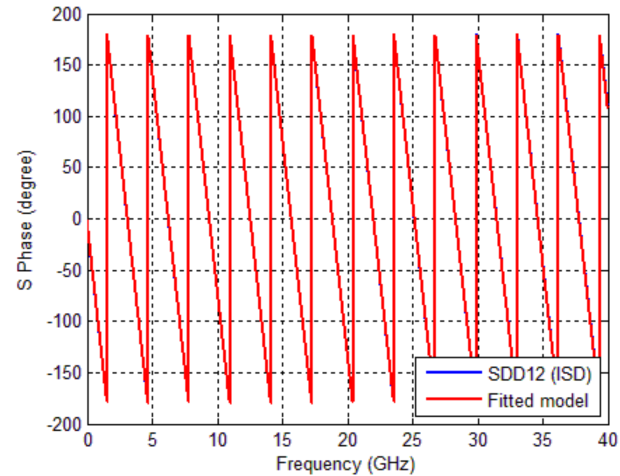
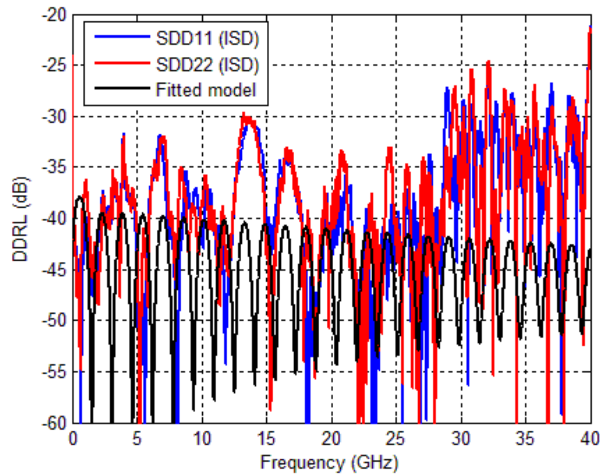
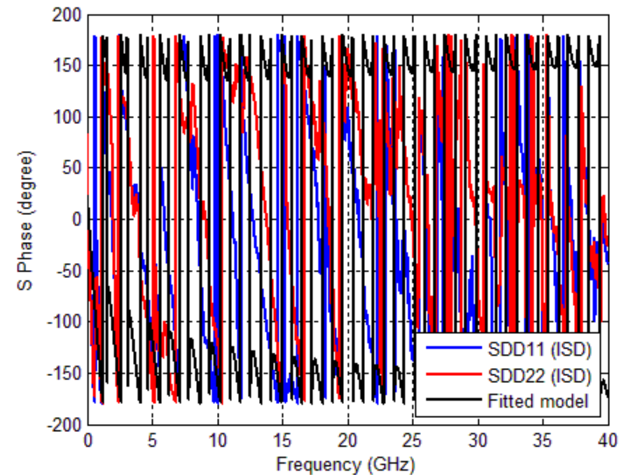
DDIL and DDRL匹配









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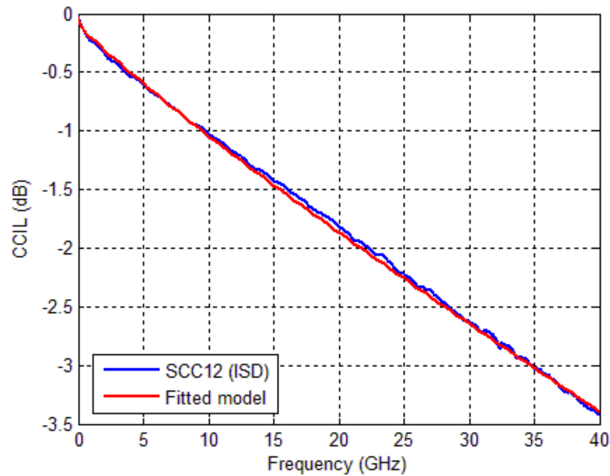
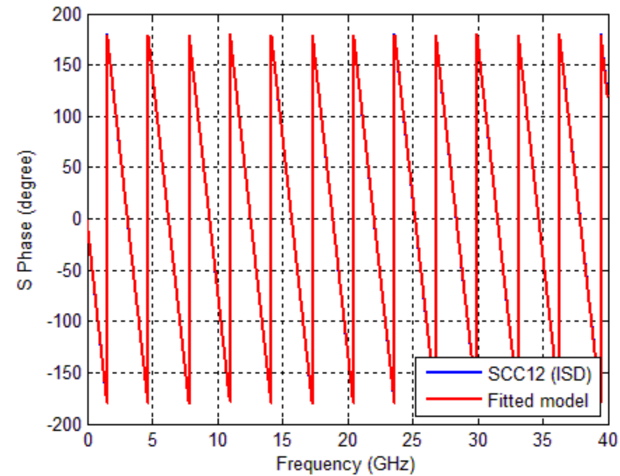
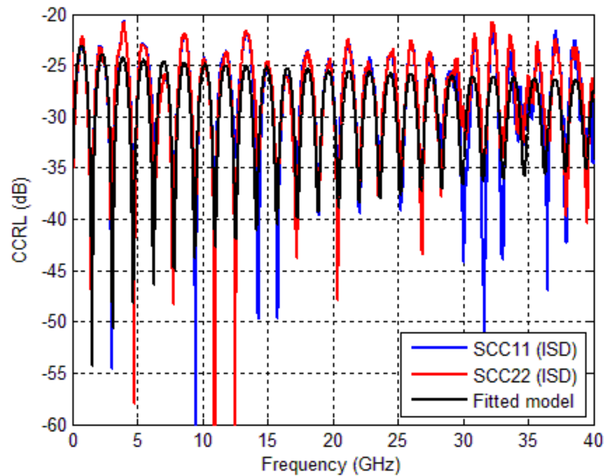
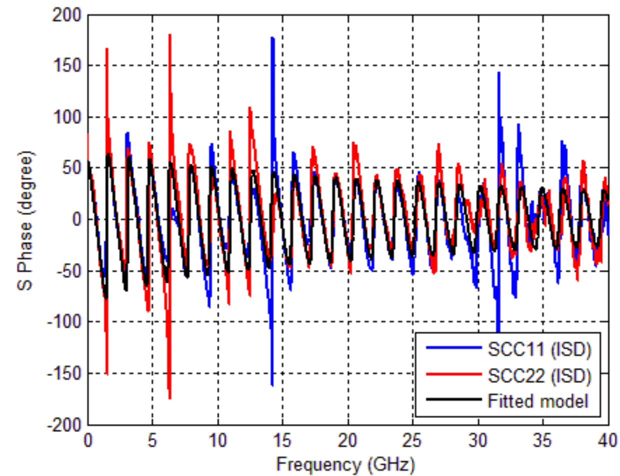
CCIL and CCRL匹配









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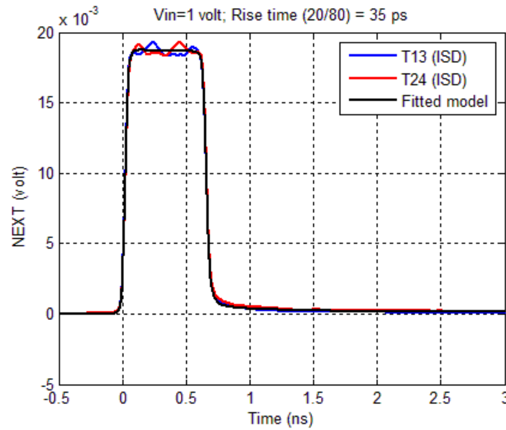
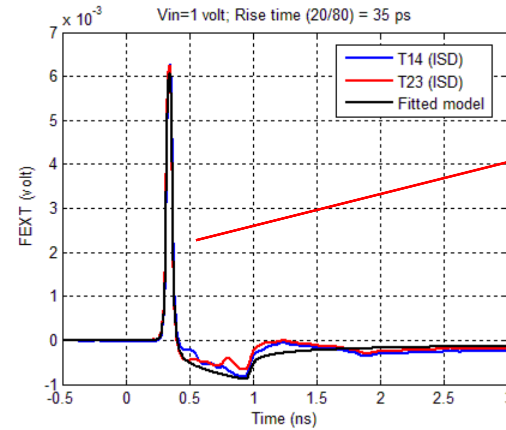
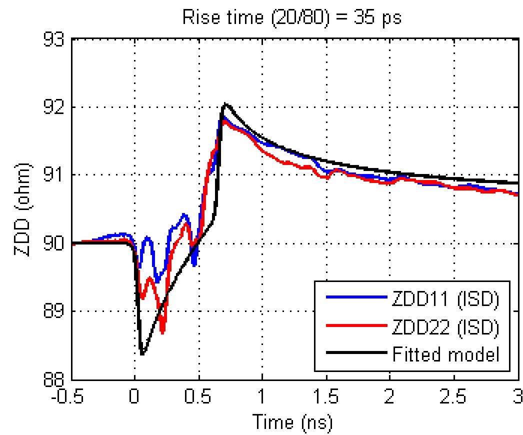
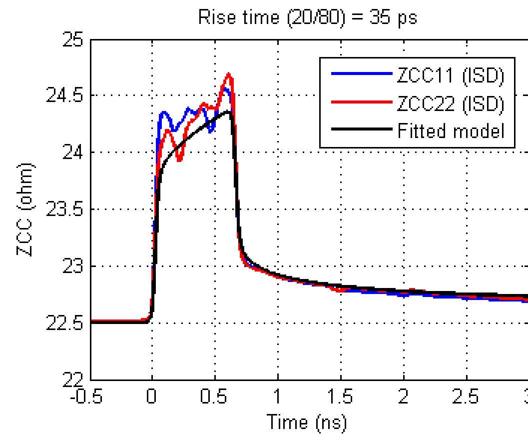
TDT and TDR匹配

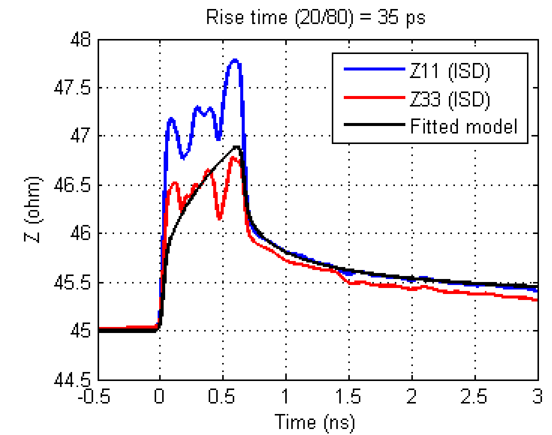




Positive polarity implies $K_C > K_L$







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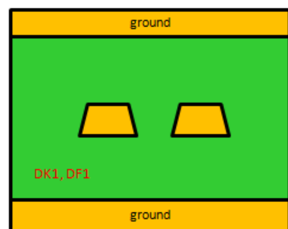
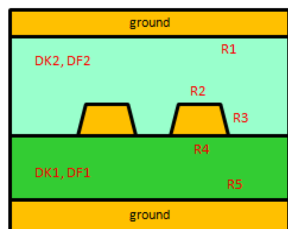
5种模型的比较

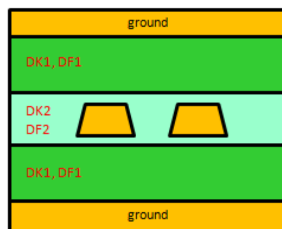
- 模型1无法匹配FEXT。模型2至5可以很好地匹配所有IL，RL，NEXT，FEXT和TDR / TDT



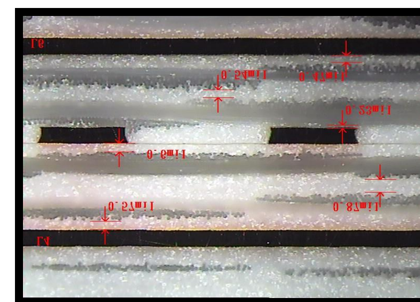
Model 1

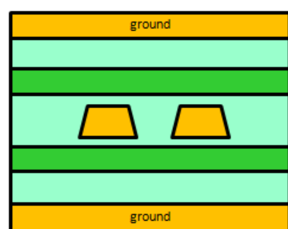


Model 2

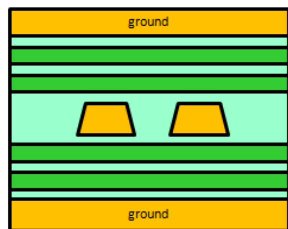


Model 3





Model 4



Model 5

DK1 DK2

Model	DK1	DK2
1	3.510	-
2	2.444	4.294
3	3.413	3.623
4	3.863	3.360
5	3.115	3.975

At 10 GHz

DK2>DK1 because of positive-polarity FEXT

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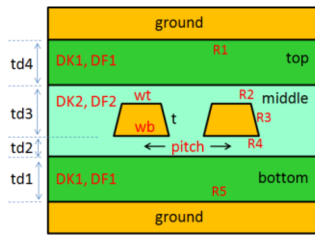
提取 DK1 和 DF1

模型3



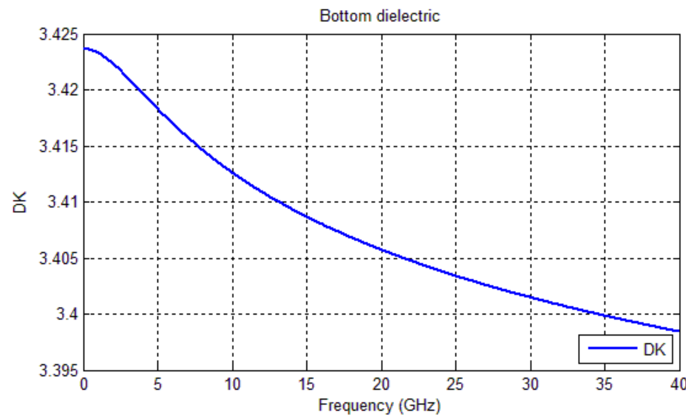
$$\varepsilon_\infty = 3.27929$$

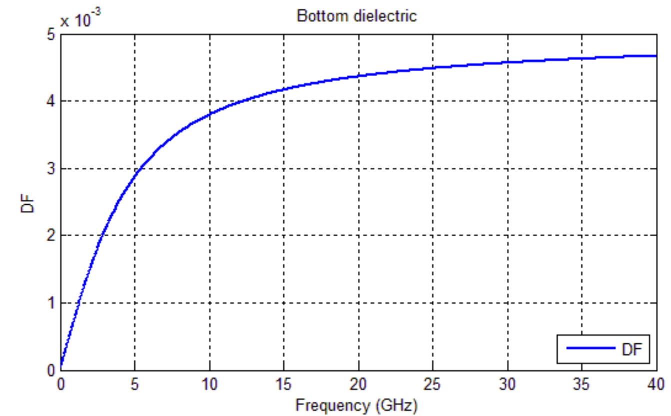
$$\Delta\varepsilon = 0.144348$$

$$m1 = 9.58619$$

$$m2 = 15.4109$$

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right) = \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$





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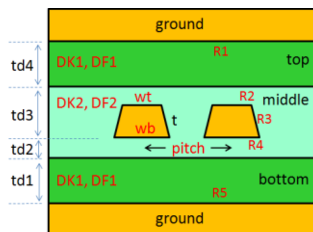
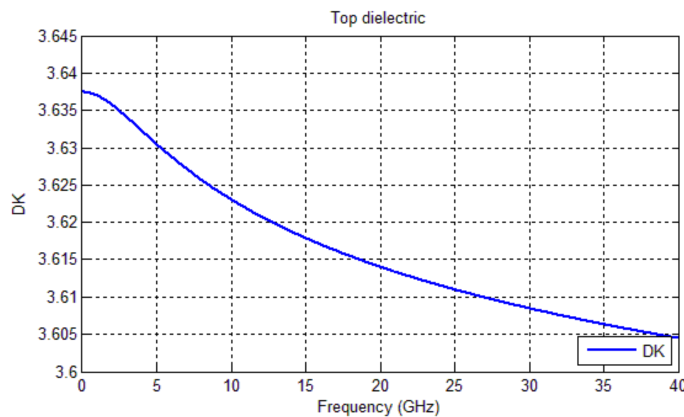
提取 DK2 和 DF2

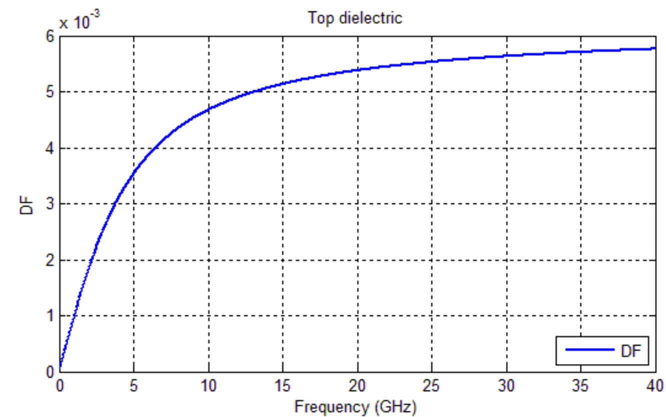
模型3



$$\varepsilon_\infty = 3.46724$$
$$\Delta\varepsilon = 0.170196$$
$$m1 = 9.58715$$
$$m2 = 14.8352$$

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$





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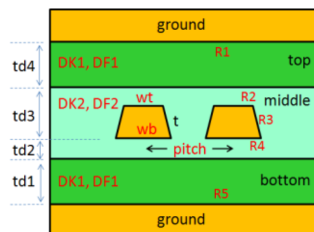
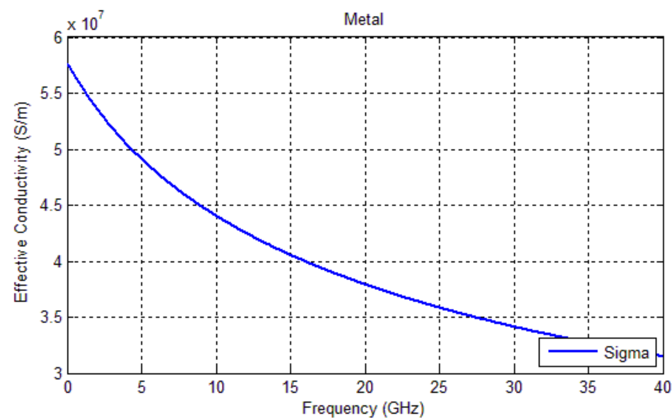
提取有效电导率

模型 3

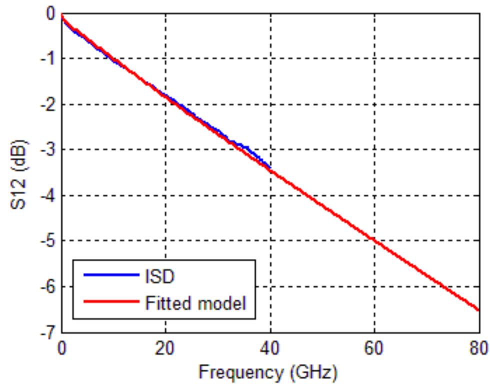


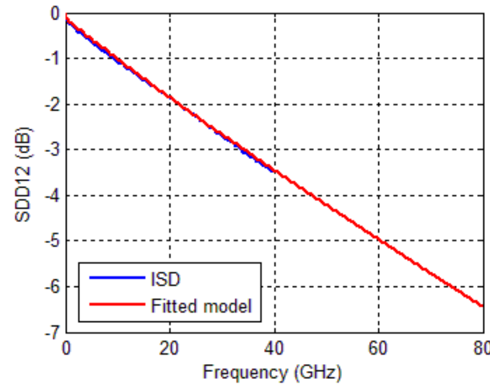
$$\sigma = 5.8 \times 10^7 \text{ S/m}$$

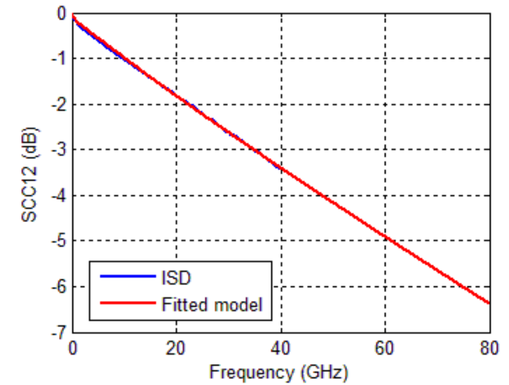
$$R_q = 0.324321\, \mu\text{m}$$

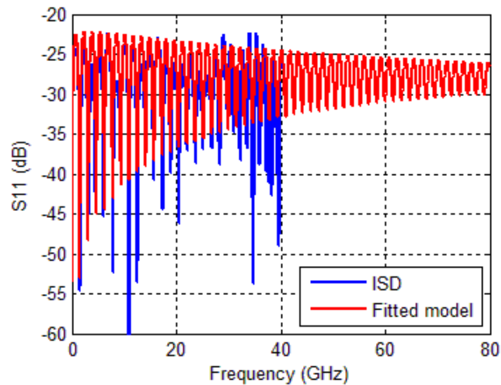


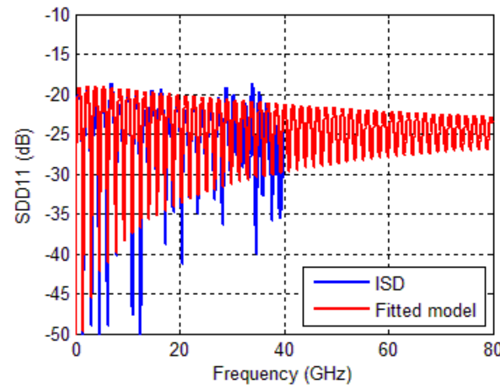
可以创建长度和频率可缩放的模型.

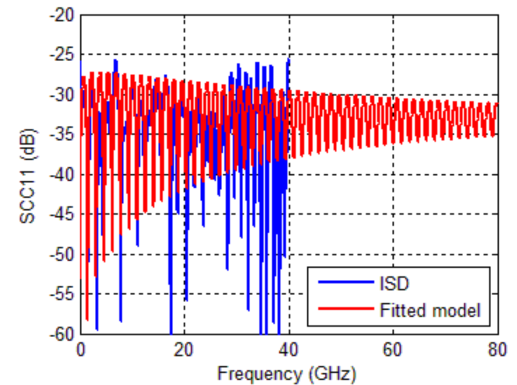












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Summary

- 准确的去嵌入对于设计验证，一致性测试和PCB材料属性（DK，DF，粗糙度）提取至关重要。
- 如果测试夹具和校准结构具有不同的阻抗，则传统的去嵌入方法会在被测设备（DUT）结果中产生非因果错误。
- 原位去嵌入（ISD）通过软件而非硬件解决了此类阻抗差异，从而提高了去嵌入精度，同时降低了硬件成本。

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